GALLIUM NITRIDE SUPERJUNCTIONS FOR POWER ELECTRONIC APPLICATIONS

A Dissertation

by

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ABSTRACT

Gallium Nitride (GaN) is a wide-band gap semiconductor that has found market acceptance in applications such as lighting, power electronics and radio-frequency electronics. The high breakdown electric field and electron saturation velocity of GaN are favorable relative to Silicon, but manufacturing costs and material defects have limited the market penetration of GaN. Commercial GaN devices are based on a two-dimensional electron gas (2DEG) that arises from spontaneous and piezoelectric polarization at the hetero-interface between GaN and Aluminum Gallium Nitride (AlGaN). These 2DEG-based devices, termed High Electron Mobility Transistors (HEMTs), have under-performed to date when comparing semiconductors with the Baliga Figure of Merit (BFOM) for power electronics. However, Silicon and Silicon Carbide (SiC) devices have exceeded their respective material limits due to lower defect density materials and device engineering. Currently, no native substrate for GaN is economically viable or commercially available so Group III-Nitrides are deposited on Si, Sapphire or SiC. This hetero-epitaxy leads to high defect densities in the epitaxial films which hinder device performance and reliability. Therefore, the reduction of defect densities and manufacturing costs is critical to meeting goals set-forth by government agencies to improve power conversion efficiencies while being cost competitive.

The work presented herein provides a potential solution to manufacturing low defect density GaN devices that have both a low on-state resistance, R_{ON} and high blocking voltage capability, V_{BR}, on Silicon substrates. This is accomplished by utilizing selective area epitaxy (SAE), which reduces the defect densities of the epitaxial films, and adopting the superjunction (SJ) device architecture from Silicon that reduces the engineering trade-off between R_{ON} and V_{BR}. A SJ device requires n-type and p-type GaN materials (n-GaN and p-GaN, respectively), of which p-GaN has proven to be a material that is difficult to achieve in low resistivities. However, the doping ranges required to achieve high voltage operation have been frequently demonstrated. The SAE process requires extra lithography and deposition steps relative to a commercial GaN-on-Si HEMT technology, therefore the high growth rates of the SAE are leveraged to reduce deposition time and

thinner buffers layers could enable larger wafer diameters.

Parametric device simulations are presented to determine which design parameters are most sensitive in the superjunction process. The SJ layer charge and metal contact resistance to the p-GaN were found to be the two most critical design parameters. Next, an epitaxial GaN process was developed on sapphire substrates using Metal Organic Chemical Vapor Deposition (MOCVD). The GaN-on-Sapphire films were characterized using Hall measurements and diodes to understand the background doping concentration of the unintentionally doped GaN (UID-GaN). These GaN films and devices serve as a baseline for comparing GaN films grown on Silicon substrates. Integration of GaN with Silicon control electronics is an attractive technology to reduce interconnect losses and minimize footprint. However, commercial GaN devices are grown on Silicon (111) substrates while CMOS devices are fabricated using Silicon (100). A GaN-on-Silicon (100) process was developed using Atomic Layer Deposition (ALD) Aluminum Oxide (Al_2O_3) as a nucleation layer, with the goal of understanding how GaN could be grown on Silicon (100) substrates to avoid costly bonding and substrate removal processes. X-ray Diffraction (XRD) and electrical characterization was utilized to compare the GaN quality between Silicon substrates and the GaN-on-Sapphire. A SAE process for GaN on Sapphire substrates was developed using a Plasma Enhanced CVD (PECVD) Silicon Nitride (Si_3N_4) dielectric as a mask. Scanning Electron Microscopy (SEM) was utilized to monitor lateral epitaxy and provide information on how to control the film morphology. Significant defect density reduction of the SAE GaN films was accomplished by using Aspect Ratio Trapping (ART), which is a form of SAE where the aspect ratio of the dielectric window is greater than 1. Electron beam lithography (EBL) and Reactive Ion etching (RIE) processes were developed to obtain an aspect ratio of 1.2. Transmission Electron Microscopy (TEM) was then performed on the ART GaN-on-Silicon (111) which verified defect trapping inside the windowed region. Lastly, p-GaN ohmic contacts were developed using Nickel and Gold as a baseline process. Improvements to the baseline ohmic contact process was made by using Magnesium as an inter-layer between the p-GaN and the Nickel.

DEDICATION

To my father.

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NOMENCLATURE

2DEG	Two-dimensional electron gas
ALD	Atomic Layer Deposition
AlGaN	Aluminum Gallium Nitride
Al_2O_3	Aluminum Oxide
ART	Aspect Ratio Trapping
BFOM	Baliga Figure of Merit
BOE	Buffered Oxide Etch
DI	De-ionized Water
EBL	Electron Beam Lithography
FWHM	Full Width at Half Maximum
GaN	Gallium Nitride
HEMTs	High Electron Mobility Transistors
LTVGR	Lateral-to-Vertical Growth Rate
MOCVD	Metal Organic Chemical Vapor Deposition
n-GaN	n-type GaN
PECVD	Plasma Enhanced Chemical Vapor Deposition
p-GaN	p-type GaN
RIE	Reactive Ion Etching
R_{ON}	On-state Resistance
SAE	Selective Area Epitaxy
SEM	Scanning Electron Microscopy
SiC	Silicon Carbide

Si_3N_4	Silicon Nitride
SJ	Superjunction
TEM	Transmission Electron Microscopy
UID-GaN	Unintentionally Doped GaN
V_{BR}	Breakdown Voltage
WBG	Wide Band-Gap
XRD	X-ray Diffraction

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1. INTRODUCTION

1.1 Motivation and Power Electronics

Power electronic systems control and convert electrical energy for industrial, commercial and residential applications. Efficient conversion of electricity for these sectors is critical to minimize energy consumption which is estimated to increase 15% to 14.6 quadrillion BTUs (quads) by 2040 [1]. Moreover, projections suggest that 80 % of electricity in the U.S. will pass through a power electronic system by 2030, a significant increase from the 30% today [2]. Therefore, these systems should convert electricity efficiently to meet U.S. energy goals. A significant source of loss in a power electronic system is the semiconductor-based transistor or diode used to regulate or rectify signals [3] [4]. An engineering trade-off exists between the conductivity of a semiconductor and the maximum voltage the material can withstand before failure. Clever electron device design reduces this engineering trade-off but such devices have only been manufactured using Silicon. Significant improvements to power electronic systems could be realized if the cleverly designed devices are properly applied to materials that are more suited to power electronics applications than Silicon at an affordable price point.

Silicon-based electronics, the incumbent technology, struggle to meet demands of new power electronic systems to be smaller, more efficient and less expensive. Operating temperature limitations, high electrical conversion losses and low switching frequencies restrict the utilization of Silicon. Power electronic devices based on wide band-gap (WBG) materials, such as SiC and GaN, have entered the market [5] and demonstrated system level improvements relative to Silicon [6] [7], but manufacturing costs and reliability concerns hinder their adoption. The total available market for discrete components and modules in power electronics applications generated $11.4B in 2014 with a projected compound annual growth rate (CAGR) of 6.9 % through 2019. WBG semiconductors, SiC and GaN, accounted for 3.1 and 1.2 % of sales respectively, summing to a serviceable available market of $515MM. The target markets for the proposed technology are En-

ergy, Industrial and Automotive and Computing and Entertainment which generated $378MM in sales for WBG materials. This market information is presented in Figure 1.1(a).

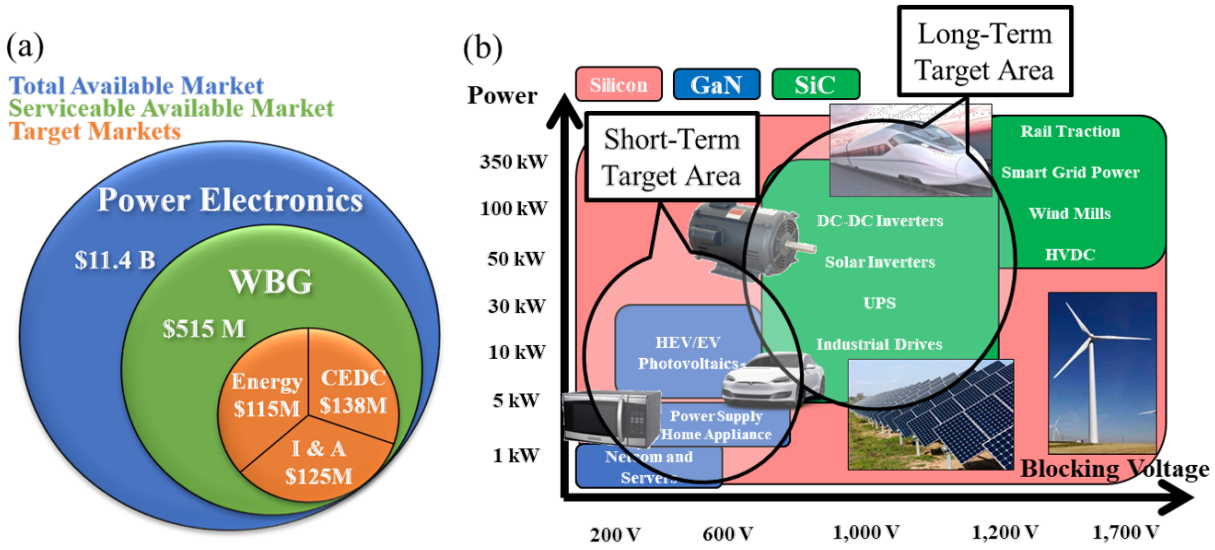

Figure 1.1: (a) Total Available Market, Serviceable Available Market and Target Markets for WBG Materials in Power Electronics and (b) current market overview for WBG and Silicon power electronics technologies (adapted from Coffa, 2015). CEDC and I&A are abbreviations of Consumer Electronics and Data Centers and Industrial and Automotive, respectively.

Currently, SiC has found market acceptance for applications requiring > 650V with GaN being the material of choice for lower voltage applications [8] as shown in Figure 1.1(b). The short-term and long-term target areas for the proposed technology are the 200 - 600 V range and the 1,000 - 1,200 V range respectively as shown in Figure 1.1(b). Research is underway to improve WBG materials and their associated devices such that they become cost competitive with Silicon. There are many companies and universities with research programs that are focused on improving power electronics, specifically through the utilization of WBG semiconductors. Three notable programs are PowerAmerica, ARPA-E SWITCHES and PNDIODES that are funded by the United States Department of Energy. PowerAmerica provides a road map for SiC and GaN commercialization. Consisting of 28 industry members, 15 university partners, 3 national labs and with current project funding of 140MM, their objective is to reduce manufacturing costs and perceived risk associated

with wide-band gap technologies. The ARPA-E project PNDIODES (Power Nitride Doping Innovation Offers Devices Enabling SWITCHES) specifically focuses on doping nitride materials for power applications, which compliments the SWITCHES (Strategies for Wide Band gap, Inexpensive Transistors for Controlling High-Efficiency Systems) program. Combined, these two programs are consist of 10 industry members, 9 universities and two laboratories. Their mission is to utilize GaN to enable more energy efficient power electronics for improved reliability and security for the electrical grid, adaptation of renewable energy sources into the grid and reduction of electricity consumption. These programs highlight to significance of improving power electronics with WBG semiconductors.

1.2 Background

The benefits of replacing Silicon power electronics with WBG semiconductors are shown in Figure 1.2. A reduction in resistive and switching losses enables improved system level efficiencies, while lower system cost is enabled due to higher switching frequencies [6] and smaller heat seaks. Improvements in power density [9] arise from larger critical electric fields for WBG semiconductors and smaller passive components due to increased switching frequency. These improvements to power electronic systems are made possible by the fundamental material properties of WBG semiconductors.

A comparison of the material properties for Silicon, SiC and GaN is shown in Table 1.1 with relevant figures of merit for power electronics [10]. The larger band gap of SiC and GaN result in a breakdown electric field that is an order of magnitude greater than that of Silicon. This allows for smaller semiconductor devices made from WBG materials for the same voltage rating, therefore reducing form factor. The listed electron mobility for GaN is based solely on the semiconductor, not on the HEMT devices that enable electron mobilities in the range of 2,000 cm^2/Vs. GaN HEMTs have become as prevalent alternative to Silicon for low voltage power electronics that switch at higher frequencies. The higher electron mobility reduces conversion losses and enables an increase in switching frequencies, therefore reducing the size of passive components and form factor. The higher thermal conductivity allows the WBG semiconductors to operate at higher

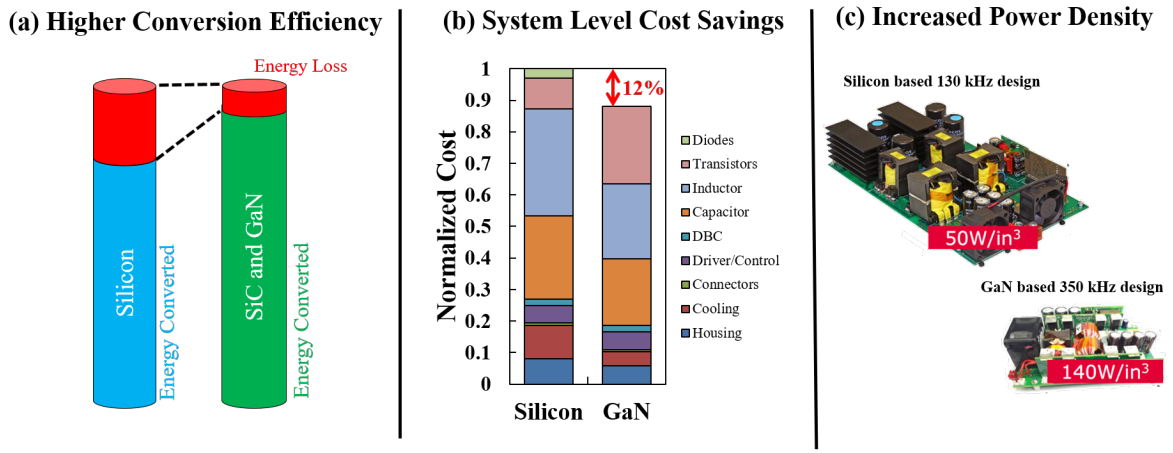

Figure 1.2: (a) Improved conversion efficiency when utilizing WBG materials (b) Cost savings on Bill of Materials (BoM) when utilizing GaN over Si, 5 kVA UPS BoM Analysis (adapted from GaN Systems, 2017) (c) Increased power density by increasing operation frequency when using GaN, 3 kW 380V – 54V Converter (adapted from McDonald, 2016).

junction temperatures increasing reliability and potentially removing the need for heat sinks in some applications.

Semiconductor Properties	Silicon	4H-SiC	GaN
Band Gap (eV)	1.1	3.3	3.4
Dielectric Constant	11.8	10.1	9
Breakdown Field (MV/cm)	0.25	2.2	3.0
Electron Mobility (cm^2/Vs)	1,500	1,000	1,250
Thermal Conductivity (W/mK)	150	490	230
Relative BFOM	1	220	630
Relative BHFFM	1	35	83

Table 1.1: Comparison of Wide-band Gap Semiconductor properties to Silicon for Power Electronics applications.

SiC has a much greater thermal conductivity than Silicon and GaN, making it ideal for high power applications. Commercial substrates of SiC exist, which enables improved thermal dissipation during high power operation, whereas a native substrate for GaN is currently not economical. Therefore, high power operation is not feasible due to the relatively poor thermal conductivity of

Silicon substrates on which GaN HEMTs are commercially available. The two figures of merit listed are the Baliga Figure of Merit (BFOM) [11] and the Baliga High Frequency Figure of Merit (BHFFM) [12] and are related to the semiconductor material properties by:

$$BFOM = \varepsilon \mu_e E_C^3 \tag{1.1}$$

$$BHFFM = \mu_e E_C^2 \tag{1.2}$$

where ε is the dielectric constant of the semiconductor, μ_e is the electron mobility and E_C is the critical breakdown field for the semiconductor.

1.2.1 Material and Device Physics

Group III-Nitride (GaN, InN, AlN) semiconductors have a wurtzite crystal structure, shown in Figure 1.3(a) which exhibits spontaneous polarization along the c-axis (0001). This polarization arises from dipole formation caused by the asymmetric wurtzite structure and the electro-negativity difference between the Group III and Nitrogen atoms. Lattice mismatch and thermal strain in the III-Nitrides lead to piezoelectric polarization that can be in the same direction as the spontaneous polarization. The deposition of Aluminum Gallium Nitride ($Al_xGa_{1-x}N$) on GaN, referred to as AlGaN/GaN, serves as the core hetero-structure utilized in High Electron Mobility Transistors (HEMTs). Differences in the total polarization between the two films and surface states are believed to be responsible for the formation of a two-dimensional electron gas (2DEG) at the interface of the GaN as shown in Figure 1.3(b) [13] [14]. This 2DEG acts as a normally-on conducting channel that exhibits high mobility (2,000 cm^2/Vs) and sheet carrier concentrations (>10^{12} cm^{-2}). The simplified band diagram for a AlGaN/GaN hetero-structure is shown in Figure 1.3(c). Commercial GaN HEMTs, shown in Figure 1.3(d), are based on this hetero-structure and resulting 2DEG.

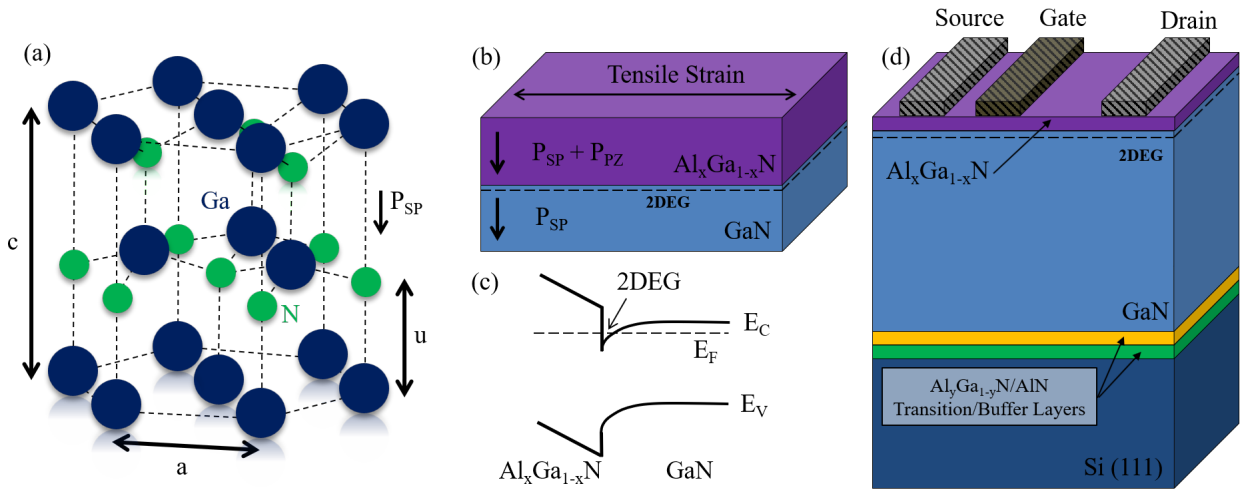

Figure 1.3: (a) Wurtzite crystal structure of GaN showing the spontaneous polarization, P_{SP}, for a Ga-polarity film. (b) $Al_xGa_{1-x}N$/GaN hetero-structure showing the P_{SP} and piezoelectric polarization, P_{PZ} for the $Al_xGa_{1-x}N$ layer due to tensile strain. (c) a simplified band diagram of the $Al_xGa_{1-x}N$/GaN hetero-structure showing the 2DEG. (d) a simplified cross-section of a GaN-on-Silicon (111) HEMT

1.2.2 Relevant Literature

State-of-the-art power devices from Silicon, SiC and GaN are shown in Figure 1.4. Commercial GaN-on-Si technology, based on HEMTs, suffer from current collapse, do not exhibit avalanche breakdown and have not demonstrated voltage handling capabilities over 650V. Additionally, HEMTs are inherently normally-on and require either a trade-off in performance or a Silicon transistor to achieve normally-off operation, significantly increasing energy conversion losses. Silicon and SiC, however, have exceeded their material limits due to device engineering [15]. These devices, Superjunctions (SJs) and Insulated Gate Bipolar Transistors (IGBTs), require a p-type and n-type film of the semiconductor to enable a reduction in the trade-off between on-state resistance and breakdown voltage. The GaN HEMT was commercially available before a suitable p-GaN material was available, but recent advances in manufacturing have seen p-GaN included in HEMT technologies. However, GaN-on-Si HEMTs continue to under perform while expensive [16] bulk GaN devices show promising performance [17]. Therefore, a need exists for GaN devices that can perform near or beyond its material limit at an affordable price. This disser-

tation begins the development for a novel GaN technology such that this need is met.

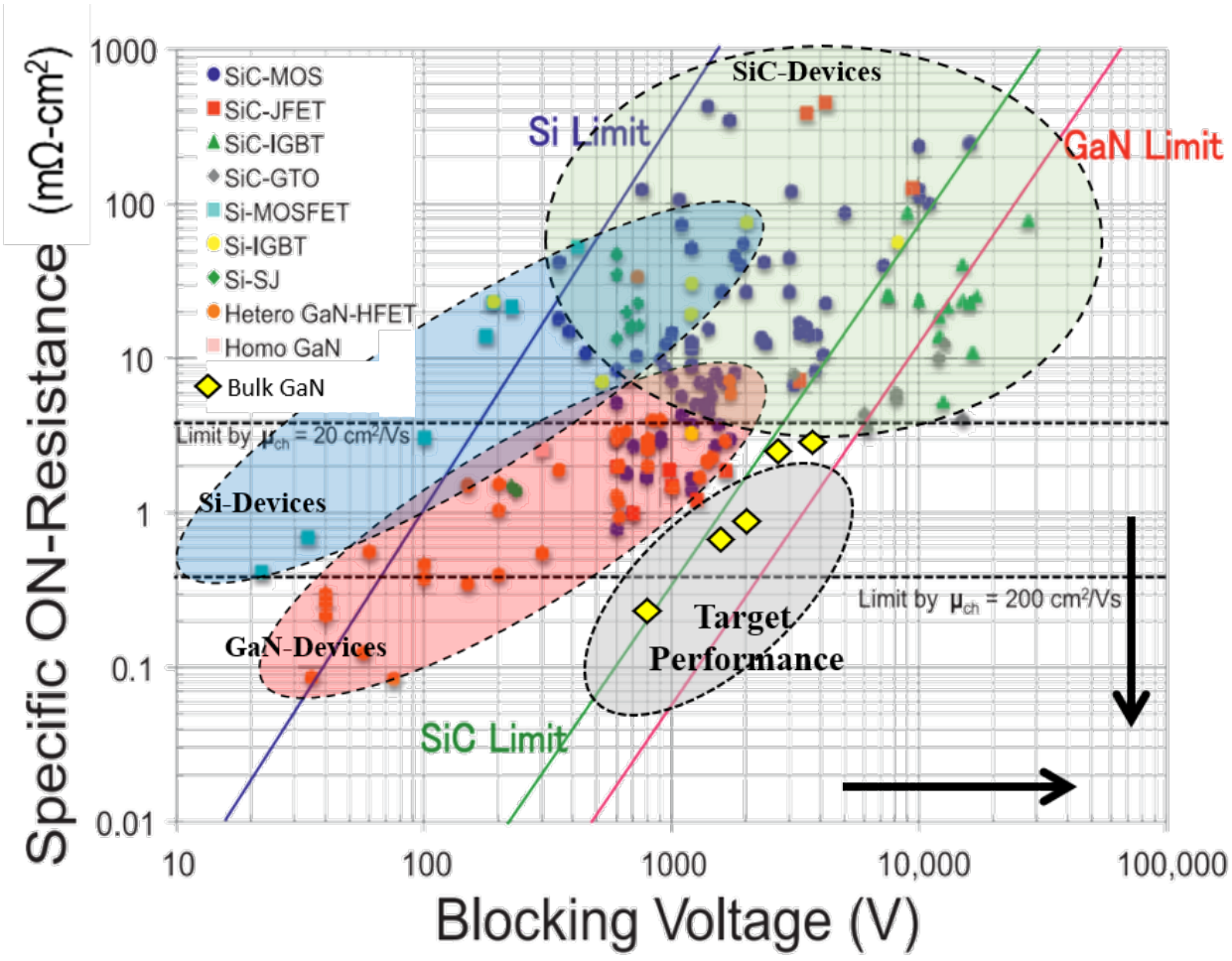

Figure 1.4: Baliga Figure of Merit for current state-of-the-art power devices from Silicon and WBG materials (adapted from Coffa, 2015)

Through unique processing steps, the proposed GaN technology addresses the problem of manufacturing low-defect density power devices with low R_{ON} and high V_{BR} on Si substrates. Full deployment of this technology would enable significant energy savings, estimated at 1.3 quads per year [18], and allow for a two-fold increase in power density while reducing system costs by >10%.

2. PROPOSED TECHNOLOGY

The goal of this research is to provide fundamental steps and knowledge towards realizing a GaN-based SJ diode that can improve the efficiency of power electronic systems while minimizing manufacturing cost and form factor. A cross section of the proposed GaN SJ diode is shown in Figure 2.1(a) with a simplified cross-section of a vertical SJ diode based on Silicon in Figure 2.1(b). To minimize manufacturing cost, Si (111) substrates were utilized with nitride-based transition and buffer layers that enable high-quality GaN-on-Si films. The GaN-on-Si (111) wafers discussed later in this dissertation were obtained from Texas State University and were used as a starting material for the ART GaN process. This proposed technology is unique due to the combination of SAE and a SJ device architecture applied to GaN. The majority of the research presented herein is focused on developing proper SAE of the GaN structure and the development of ohmic and schottky contacts to p-GaN and n-GaN.

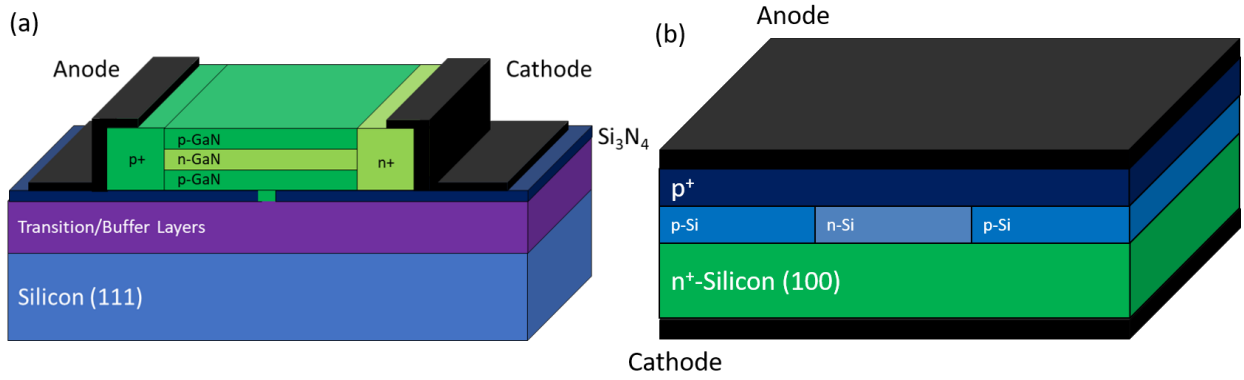

Figure 2.1: (a) Cross-section of the proposed lateral GaN superjunction technology (b) cross-section of a simplified vertical Silicon superjunction.

The SJ structure allows for a reduction in the engineering trade-off between V_{BR} and R_{ON} of a power device [19]. Furthermore, the utilization of SAE enables the GaN films to have dislocation densities 2-3 orders of magnitude lower than the underlying GaN films [20] [21]. This enables

lower leakage currents [22] which reduces conversion losses in the off-state. The goals of this research are outlined in Table 2.1. The window aspect ratio goal corresponds to the geometry of a window etched in the Silicon Nitride mask for SAE. An aspect ratio of greater than one has been shown to aid in the trapping of defects for a variety of semiconductors, including GaN [23] [24] [25]. The GaN XRD Full Width at Half Maximum (FWHM) goal is specified for the baseline GaN-on-Sapphire process. The contact resistance, R_C, to n-GaN and p-GaN is an important metric for minimizing the total R_{ON} of the SJ structure as will be shown in simulations.

Metric	Goal
Window Aspect Ratio	> 1
GaN XRD FWHM (002)	< 500 arcseconds
n-GaN R_C	$< 10^{-5}\ \Omega - cm^2$
p-GaN R_C	$< 10^{-4}\ \Omega - cm^2$
Diode R_{ON}	$< 5\text{x}10^{-3}\ \Omega - cm^2$
Diode V_{BR}	> 200 V

Table 2.1: Metrics and goals for the research presented herein.

The development of an epitaxial GaN-on-Sapphire process serves as baseline material quality for developing a GaN process on Silicon (111) and (100) substrates. This process is then applied to Si (111) and (100) substrates with a thin ALD Al_2O_3 film to improve film quality on foreign substrates. Second, an electron beam lithography process and dry etch recipe is developed to meet the aspect ratio goal outlined in Table 2.1. Then, a SAE GaN process is developed. From these n-GaN films, ohmic contacts and diodes are fabricated. Following this device fabrication, ohmic contacts to p-GaN are developed.

There are at least three different manufacturing methods to realize the proposed GaN SJ. Figure 2.2 highlights the key steps for one of the possible manufacturing process flows with the other two process flows provided in Appendix B. The flow begins with the selection of a suitable substrate, typically Silicon (111), SiC, Al_2O_3, and any appropriate buffer/transition layers on the substrate (i.e. AlN, $Al_xGa_{1-x}N$) to enable high quality GaN growth. After the appropriate substrate

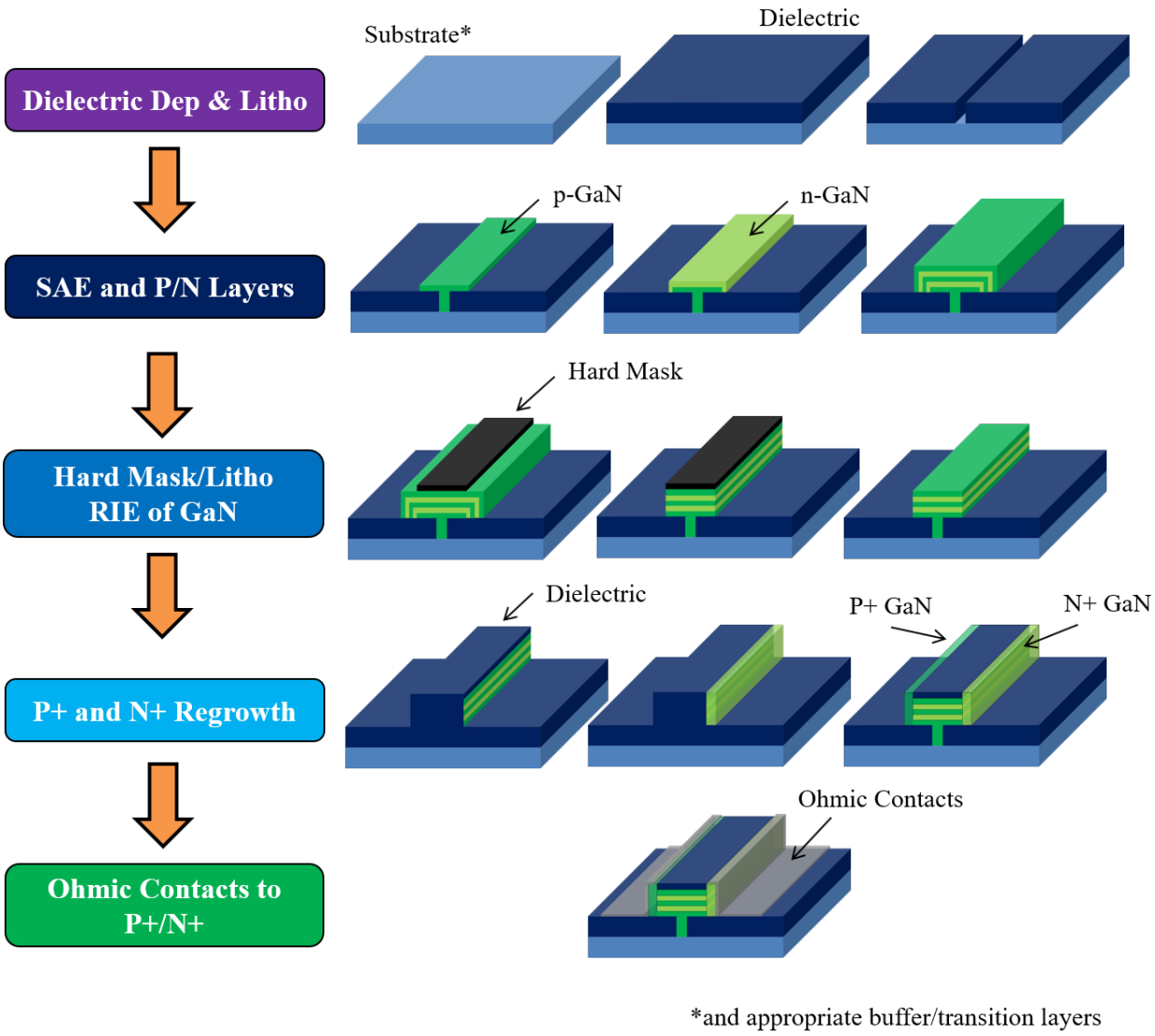

Figure 2.2: Fabrication process to realize a GaN superjunction based on selective epitaxy.

and suitable buffer/transition layers are deposited, a dielectric layer is deposited to enable selective epitaxy (i.e. Si_3N_4, SiO_2). A window is patterned in the dielectric layer, preferably with an aspect ratio greater than one to enable defect trapping inside the window. The process proceeds with selective area epitaxy (SAE) of GaN and the growth of alternative p/n layers. Figure 2.2 shows an odd number of layers superjunction channels with the first and last layer being p-type GaN. The next step involves the etching of the superjunction channels by utilizing a hard mask and reactive ion etching. The process continues with regrowth of the P+ and N+ GaN regions from the side-

walls of the GaN superjunction structure. These regions help reduce metal/semiconductor contact resistance. The final step of the manufacturing process is the deposition of the ohmic contacts to the P+ and N+ GaN regions. This process requires 6 lithography steps, 3 epitaxy steps, at least three dielectric depositions and at least one plasma etching step. The SAE process of GaN has been extensively researched with the GaN morphology and defect propagation well understood. Similarly, dry etching of GaN is well understood and is typically accomplished with Cl_2-based plasma chemistries to etch thick GaN films [26] [27]. Difficulties associated with doping GaN p-type will be discussed later along with a range of hole concentrations commonly reported. Before process development begins, the design of a superjunction using simluations is presented. The goals of the simulated superjunction performance are outlined in Table 2.2.

Metric	Goal
Diode R_{ON}	< 2x10^{-3} $\Omega - cm^2$
Diode V_{BR}	> 1,200 V
N+ GaN R_C	10^{-6} $\Omega - cm^2$
P+ GaN R_C	10^{-4} $\Omega - cm^2$

Table 2.2: Metrics and goals for designing a GaN superjunciton given contact resistances to the N+ and P+ GaN.

3. SUPERJUNCTION SIMULATIONS

Simulations of GaN superjunctions are based on HEMT structures or use polarization engineering to enable charge balance, but both structures have complex device architecture without significant V_{BR} benefit [28] [29]. To date, the impact of epitaxy process on device performance has not been properly considered. Therefore, the goal of this section is to understand how manufacturing can affect the breakdown voltage and on-state resistance of a superjunction based on GaN. A design window based on the column charge and thickness is presented based on current doping limitations of n-GaN and p-GaN. Solutions to Poisson's equation using finite element numerical simulations is used to find the conditions for breakdown, which occured the impact ionization integrals reached a value of one. The on-state resistance of each device studied was extracted from the inverse slope at a forward bias of 5V. The device cross-section of all devices studied was 1μm x 1.5μm, which was used to calculate the specific on-state resistance in mΩ cm^{-2}. To minimize contact resistance, p+ and n+ regions of 1.0x10^{18} cm^{-3} are included at the ends of the superjunction columns. A quasi-optimized device design was chosen based on the R_{ON}-V_{BR} FOM and used to study the impact of dopant diffusion and charge imbalance in SJ channels. Lastly, the impact of contact resistance to the p+ and n+ GaN on the final R_{ON}-V_{BR} FOM is presented.

3.1 Superjunction Design

Properly designing a superjunction, also known as a charge-coupled device, requires knowledge of the optimum charge based on the geometry of the device. The optimum charge Q_{OPT} [10] is related to the doping density, N_D, and the layer thickness of the GaN, W_N, by

$$Q_{OPT} = qN_DW_N = \epsilon_sE_C \tag{3.1}$$

where q is the electron charge, ϵ_s is the semiconductor dielectric constant and E_C is the critical electric field of the semiconductor. The optimum charge for GaN is 2.78x10^{-6} C-cm^{-2} given ϵ_s = 9.5 and E_C = 3.3 MV/cm [30]. This linear relationship between charge and thickness and

the cross-section of the simulated SJ (inset) are shown in Figure 3.1. Layer thickness of 500 nm (red diamond in Figure 3.1) was chosen for all subsequent SJ designs. The doping density of the column is varied in the next section from 1.0x10^{16} cm^{-3} to 5.0x10^{17} cm^{-3} to determine Q_{OPT} for the given SJ design.

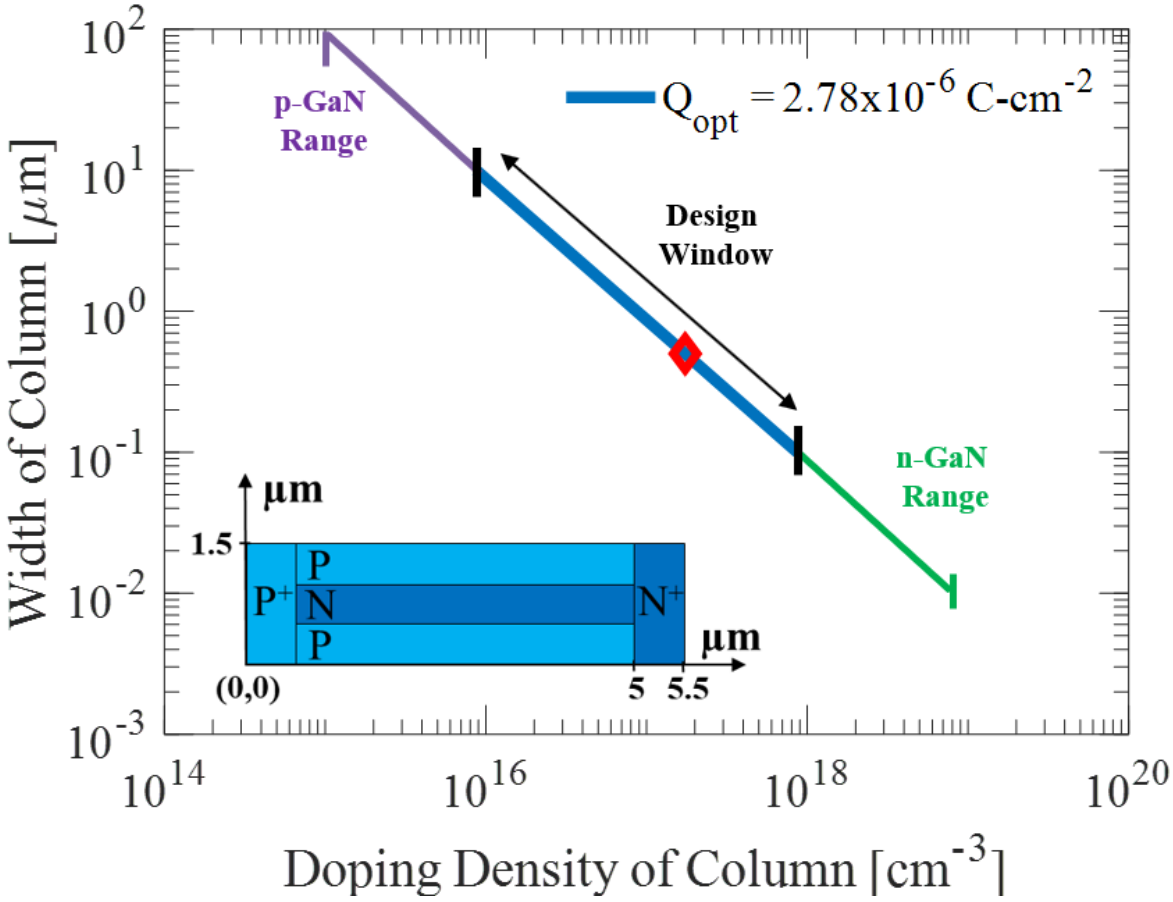

Figure 3.1: Design window for GaN superjunctions based on the optimum charge equation and a feasible doping range for n-GaN and p-GaN. The inset shows the device structure used in the presented simulations with the red diamond representing a superjunction with a column width of 500nm.

3.2 Charge-Balance Doping Variation

The impact of doping variation within the window described in Figure 3.1 was performed by varying the doping density, for both n-GaN and p-GaN regions, from 1.0x10^{16} cm^{-3} to 5.0x10^{17} cm^{-3}. The R_{ON}-V_{BR} FOM for the simulated devices is shown in Figure 3.2. The nine charge balanced devices were compared by calculating a Figure of Merit (FOM) to determine which device had the quasi-optimum layer charge:

$$FOM = \frac{V_{BR}^2}{R_{ON}}. \tag{3.2}$$

The simulated device with doping density of 2.5x10^{16} cm^{-3} had the highest FOM of 3.94x10^{10} $V^2\Omega^{-1}cm^{-2}$, which goes beyond the GaN uni-polar material limit (9.09x10^9 $V^2\Omega^{-1}cm^{-2}$). The layer charge based on this geometry and doping suggests the optimum charge to be $4.0\text{x}10^{-7}$ $C - cm^{-2}$. The difference is attributed to the presence of the p+ and n+ regions at the end of each superjunction column. For the subsequent charge imbalance studies, all structures have at least one column doping of 2.5x10^{16} cm^{-3} with all columns fixed at a thickness of 500 nm.

To understand why a specific doping concentration enabled superior R_{ON}-V_{BR} position-dependent electric field lines are plotted in Figure 3.3 for charge-balanced devices with three different doping densities at zero-bias in Figure 3.3(a-f). The electric field lines are taken along the transverse and longitudinal directions of the device, indicated by the A and B lines shown in Figure 3.3(a). The initial distribution of space-charge at equilibrium is important to produce the appropriate electric field distribution at high bias as shown in Figure 3.3(c-d). Transverse electric field distributions, shown in Figure 3.3(c), for devices with doping less than 10^{17} cm^{-3} show a depletion region that encroaches upon the center n-GaN column at zero bias. This enables full depletion to occur sooner at high bias than a column with higher doping. Alternatively, the 5.0x10^{17} cm^{-3} device has lower space charge encroachment into both n-GaN and p-GaN layers, thereby increasing the initial peak electric field which results in a non-uniform distribution of potential longitudinally as shown in Figure 3.3(d). The reduction of total space charge in the n-GaN and p-GaN layers for

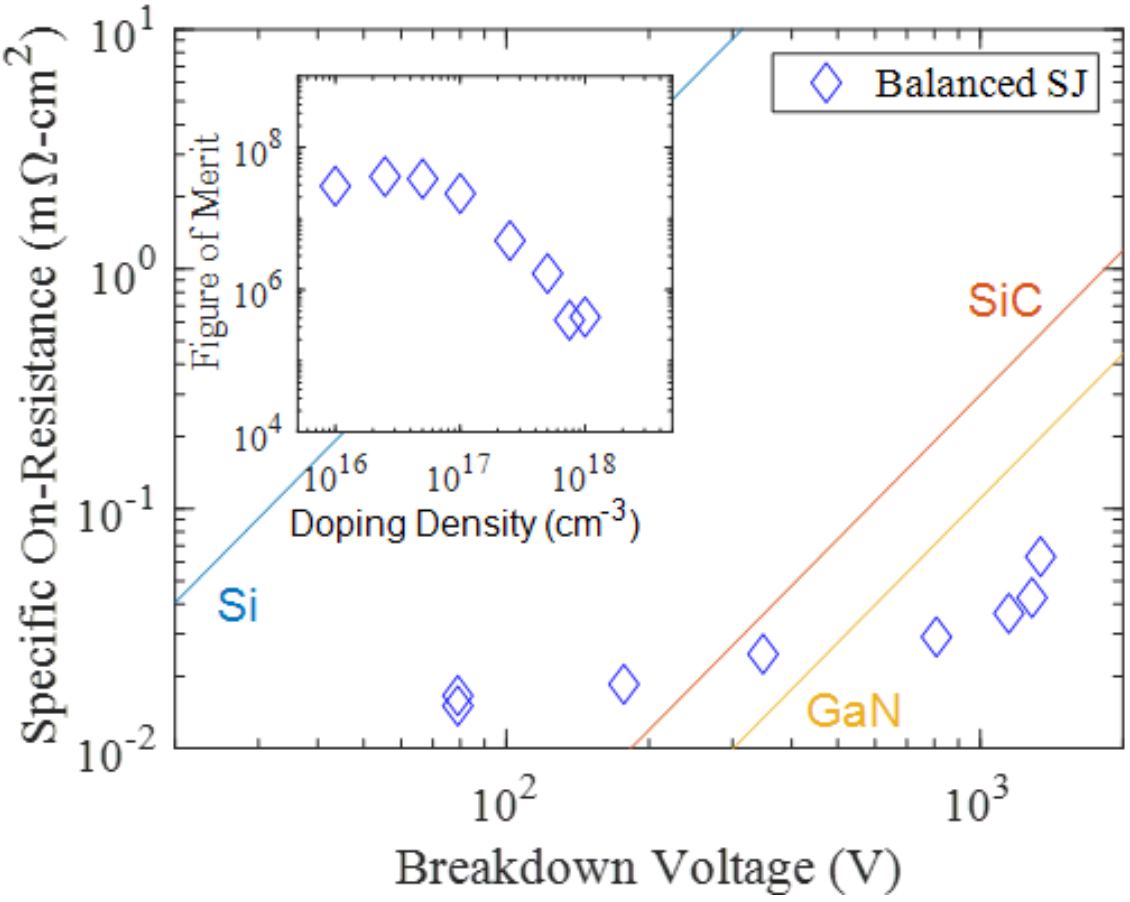

Figure 3.2: Baliga Figure of Merit for the Balanced Superjunction devices simulation. Inset is the FOM vs. Doping density plot to determine the quasi-optimum doping concentration for the studied superjunction structure.

doping densities greater than 10^{17} cm^{-3} results in a large potential drop and electric field at the n+/p junction longitudinally as seen in Figure 3.3(d). Thus, doping less than 10^{17} cm^{-3} maintains a higher baseline longitudinal electric field, thereby evenly distributing the potential at high bias. Proper depletion of the n-GaN and p-GaN layers at zero-bias results in a uniform electric field at breakdown for 1.0x10^{16} cm^{-3} and 2.5x10^{16} cm^{-3} devices, while the 5.0x10^{17} cm^{-3} device has not achieved full transverse depletion even at breakdown as shown in Figure 3.3(e). The resulting longitudinal breakdown electric field distribution, Figure 3.3(f) indicates the significant peak at the n+/p junction for 5.0x10^{17} cm^{-3}, while the lower doping density devices maintain a more even electric field variation, thus distributing the potential more uniformly along the longitudinal axis of

the device. The breakdown voltage of these three devices is 1,340V, 1,286V and 177V respectively for increasing doping. However, R_{ON} decreases monotonically with increased doping, providing the engineering trade-off between V_{BR} and R_{ON}.

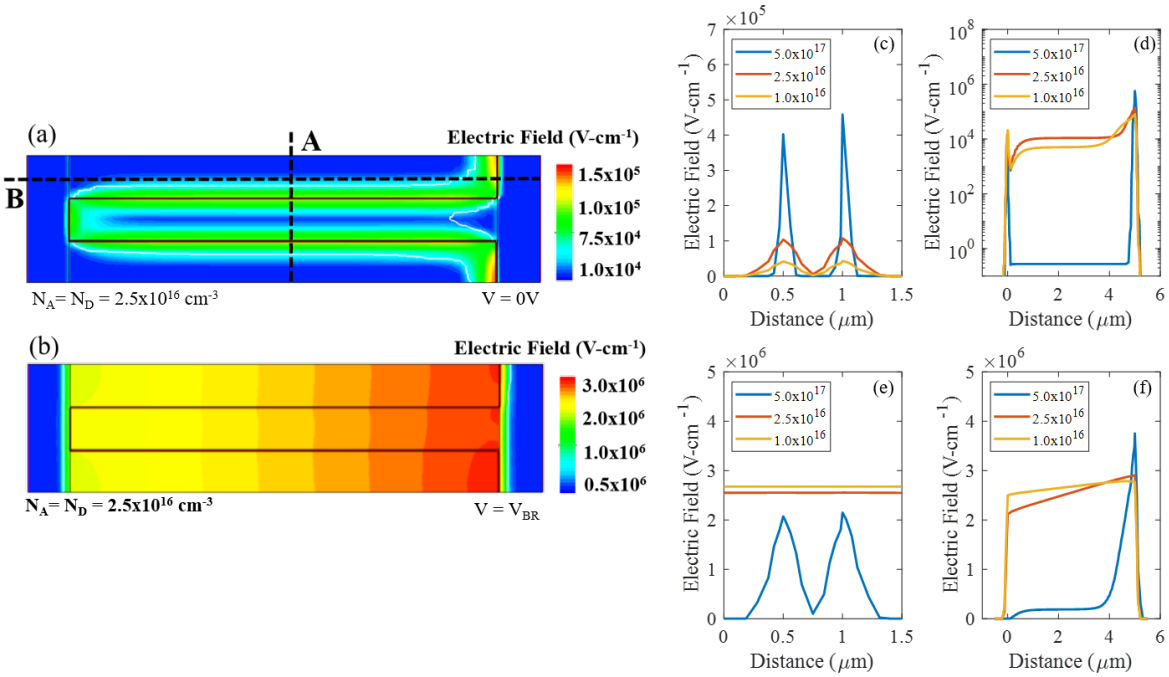

Figure 3.3: (a-b) Electric field heat maps for a charge balanced superjunction with doping of 2.5x10^{16} cm^{-3} at (a) zero-bias and (b) breakdown. (c-f) Electric field distributions along lines A and B in Figure 3(a) at (c-d) zero-bias and (e-f) breakdown.

3.3 Dopant Diffusion Impact on Figure of Merit

Manufacturing processes for GaN require high temperature which will impact dopant distributions. Therefore, it is important to understand how non-ideal dopant distribution profiles could impact device characteristics, in particular V_{BR} and R_{ON}. Incomplete removal of lattice damage makes ion implantation impractical for producing p-GaN [31], therefore in-situ doping is the preferred method for manufacturing p-GaN. Figure 3.4(a) shows the comparison of an abrupt and diffused doping profiles in the SJ. For the diffused case, each channel is given a Gaussian profile

centered in the channel with peak concentration of 2.5x10^{16} cm^{-3} and a standard deviation of σ = 0.25 μm. The breakdown voltage for the σ = 0.25 μm device increased relative to the baseline (1,286V) to 1,300V. Electric field profiles of the two devices is shown in Figure 3.4(cb-c) at their associated breakdown voltages and at zero-bias. The on-state resistances for the σ = 0.25 μm device increased relative to the baseline (0.042 mΩ cm^{-2}) and was calculated to be 0.043 mΩ cm^{-2} . This study suggests that dopant diffusion could have a negligible impact on V_{BR} and R_{ON} if considered properly in the design of the SJ. Other sources of diffusion during manufacturing include thermal anneals, dopant activation and ohmic contact formation. However, these processes operate at lower temperatures and are short in duration relative to the growth of the epi-layers. Therefore, their impact on the dopant distribution are considered to be minimal. The growth rate can be increased to reduce dopant diffusion during growth to allow for more thermal budget of the device. This study represents an estimate of dopant diffusion that could occur during material growth. Due to the minimal impact on V_{BR} and R_{ON} for the diffused profile, subsequent simulations in this study will have ideal abrupt junctions between p-GaN and n-GaN regions.

3.4 Charge-Imbalance Doping Variation

Silicon superjunctions are known to be sensitive to charge imbalance, which degrades the breakdown voltage [32]. Therefore, it is important to understand how doping variations impact V_{BR} and R_{ON}. Two different scenarios were simulated: charge imbalance within the (1) n-GaN layer (N_D) and (2) within the p-GaN layer (N_A). For each study, the charge in a given layer type is varied while the doping density of the other column type is fixed at 2.5x10^{16} cm^{-3}.

3.4.1 N_D Charge Imbalance

For the n-GaN charge imbalance study, the doping concentration was studied in the range of 8.3x10^{15} cm^{-3} to 1.0x10^{17} cm^{-3} for the n-GaN, with the p-GaN doping held constant at 2.5x10^{16} cm^{-3}. Doping of the n-GaN layer with a value of 4.6x10^{16} cm^{-3} demonstrated a quasi-optimized breakdown voltage of 1,355V, the electric field profiles of which are shown in Figure 3.5(a). The transverse and longitudinal electric fields, line A and B respectively, are shown in Figure 3.4(b-e)

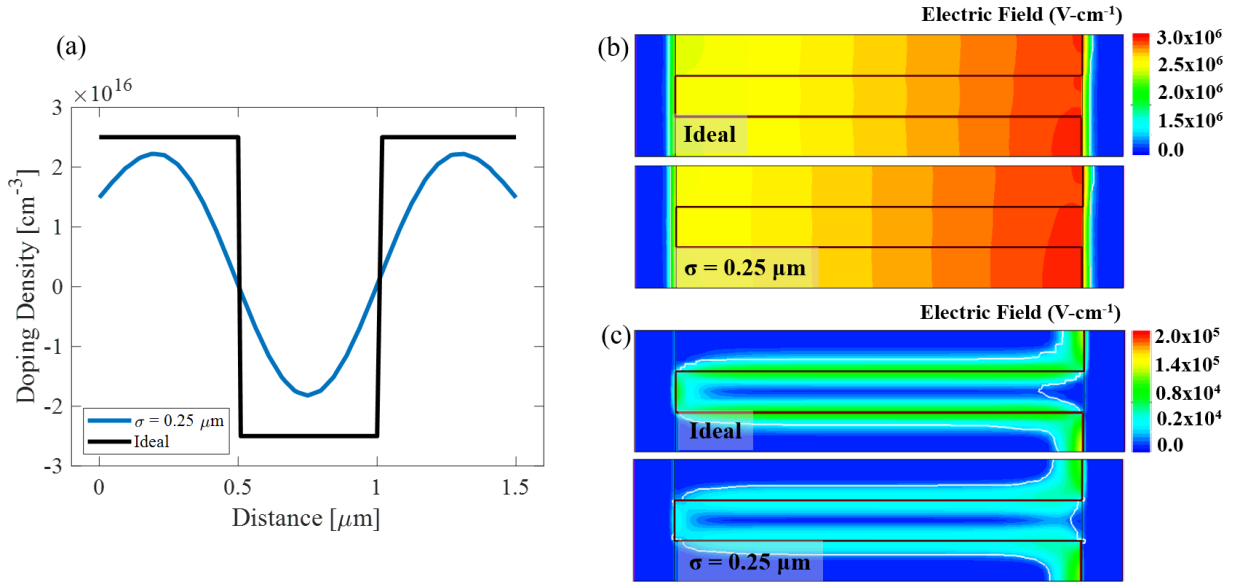

Figure 3.4: (a) Simulated dopant profiles for superjunctions with dopant diffusion based on a Gaussian distribution centered at the middle of each column with standard deviation σ = 0.25 μm. (b) Electric field profiles at breakdown for the Ideal profile (top) and the diffused profile (bottom). (c) Electric field profiles at zero bias for the Ideal profile (top) and the diffused profile (bottom).

for three different n-GaN doping values. A slight reduction in the depletion width into the n-GaN layer relative to the charge-balanced device is observed, but the more notable change is in the depletion region extension into the p-GaN and shift of peak electric field to the p+/n junction at equilibrium as shown in Figure 3.5(b). As with the charge balance study, higher doping of 1.0x10^{17} cm^{-3} leads to greater disparity in E-field from junction edge to column bulk (Figure 3.5(c)). When reverse bias is applied, this peak approaches the critical field value faster than other areas in the device leading to a reduction in V_{BR}. For the two lower n-GaN doping densities, the balanced extension of depletion regions into each column provides better distribution of equilibrium potential variation longitudinally in the n-GaN.

As seen in Figure 3.5(d), a non-uniform transverse electric field is observed at breakdown for the n-GaN doping of 1.0x10^{17} cm^{-3} and is accompanied by a peak electric field at the p+/n junction (Figure 3.5(e). However, the lower n-GaN densities provide uniform transverse electric fields which result in the electric field peak not being at the p+/n junction. For n-GaN doping densities of

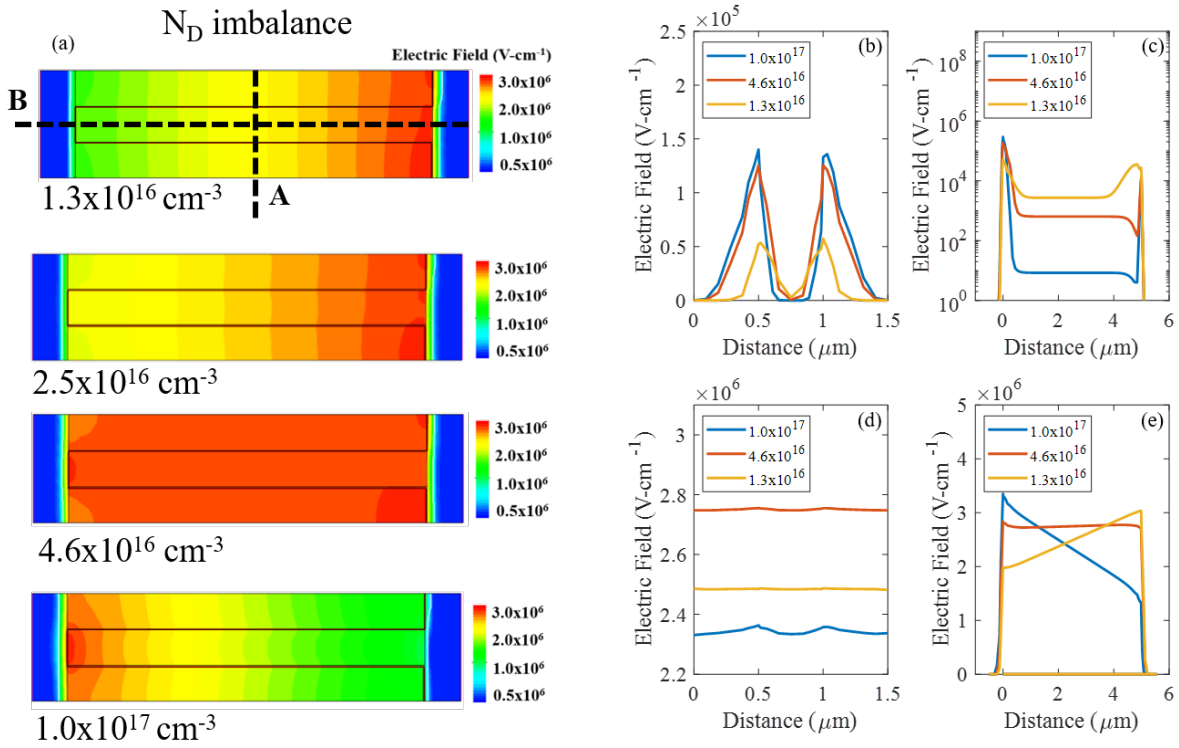

Figure 3.5: (a) Electric field heat maps at breakdown for a charge imbalanced superjunctions with doping of 2.5x10^{16} cm^{-3} for the p-GaN and the n-GaN doping density varied (b-c) zero-bias transverse and longitudinal electric field distributions and (d-e) transverse and longitudinal electric field distributions at breakdown.

less than 2.5x10^{16} cm^{-3}, the breakdown voltage was reduced. For example, the device with n-GaN doping of 1.3x10^{16} cm^{-3} shows a reduction in p-GaN depletion width at equilibrium, resulting in a non-uniform distribution of space charge during reverse bias (Figure 3.5(e)). The breakdown voltage was 1,231V for this n-GaN doping density. Breakdown occured at the p/n+ interface, which was not plotted in these figures. The trend of breakdown voltage with charge imbalance agrees with previously published studies of Silicon superjunctions. An improvement in breakdown voltage was observed for doping densities in the range of 2.5x10^{16} cm^{-3} to 7.0x10^{16} cm^{-3}. At lower doping densities the breakdown voltage was reduced slightly. For Silicon superjunctions, small charge imbalances, less than 20%, have been shown to improve breakdown voltages. However, this study concludes that GaN superjunctions with charge imbalances up to 200% in the n-GaN layer can

result in an improvement of the breakdown voltage.

3.4.2 N_A Charge Imbalance

For the p-GaN charge imbalance study, the doping concentration was studied in the range of 8.3x10^{15} cm^{-3} to 1.0x10^{17} cm^{-3} with the n-GaN doping held at 2.5x10^{16} cm^{-3}. Reducing the p-GaN layer doping to 1.3x10^{16} cm^{-3} improved V_{BR} to 1,359V, which is a similar value to the quasi-optimized device with N_D imbalance. The electric field profiles of three doping concentrations at equilibrium and breakdown for the p-GaN charge imbalance study are shown in Figure 3.6. At breakdown, the doping density of 1.3x10^{16} cm^{-3} shows a uniform distribution of the electric field throughout the structure (Figure 3.6(a)).

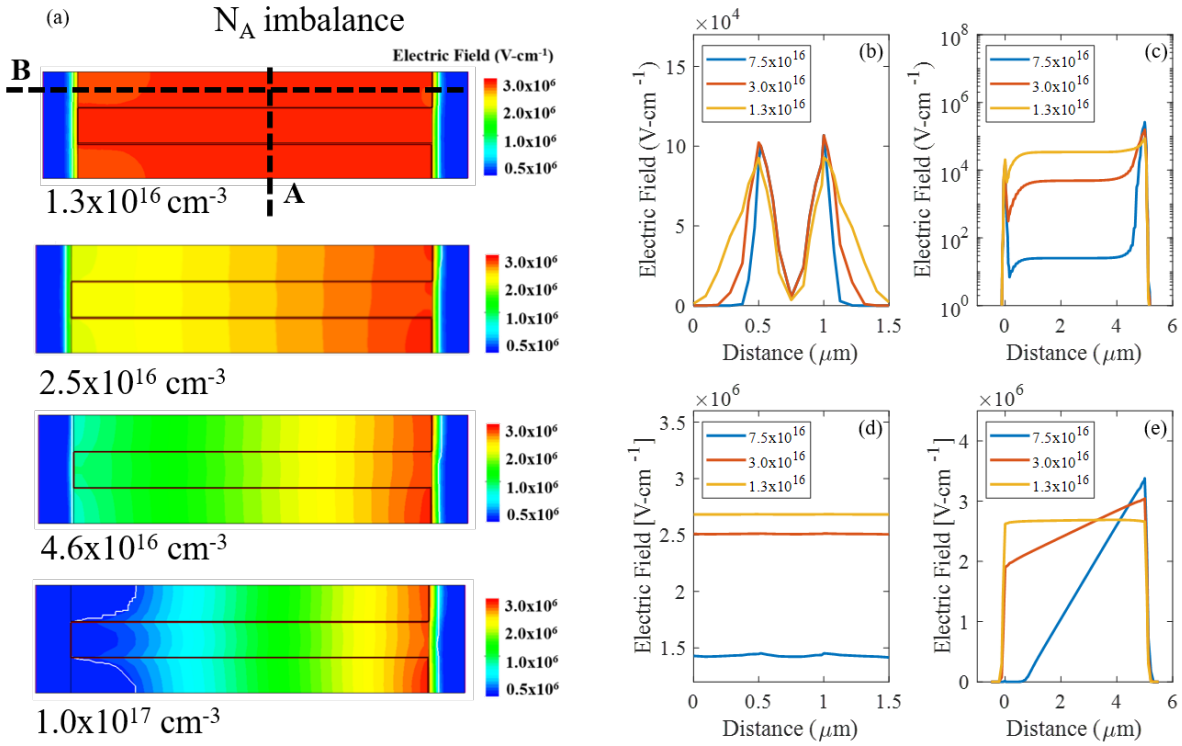

Figure 3.6: (a) Electric field heat maps at breakdown for a charge imbalanced superjunctions with doping of 2.5x10^{16} cm^{-3} for the n-GaN and the p-GaN doping density varied (b-c) zero-bias transverse and longitudinal electric field distributions and (d-e) transverse and longitudinal electric field distributions at breakdown.

Increased depletion widths into the p-GaN layers can be seen in Figure 3.6(b) at equilibrium with no discernible electric peak at any given interface. This space charge distribution at equilibrium enables a uniform potential distribution at high reverse bias which enabled an increase in the breakdown voltage. Two additional doping densities, 3.0x10^{16} cm0^{-3} and 7.5x10^{16} cm^{-3}, are shown with transverse and longitudinal electric field plots in Figure 3.6(b-e) as a comparison to the quasi-optimized device. As the doping of the p-GaN layer in increased, the depletion width into the p-GaN is reduced (Figure 3.6(b)) which decreases the bulk electric field distribution in the device (Figure 3.6(c)). The reduced depletion width leads to less transverse electric field being distributed during reverse bias (Figure 3.6(d)). The decrease of bulk electric field creates a localized electric field peak at the p/n+ interface that leads early longitudinal breakdown (Figure 3.6(e)). The breakdown voltage of the 3.0x10^{16} cm^{-3} and 7.5x10^{16} cm^{-3} devices were 1,233V and 681V respectively. The breakdown voltage was very sensitive to increases in the p-GaN layer doping, while a reduction in the doping slightly improved the breakdown voltage. These results suggest that the depletion width in the p-GaN layer is an important design parameter for the GaN superjunction. In both studies, the 3-layer superjunction of p/n/p format prefers a charge imbalance with the central n-GaN layer having higher doping than the outer two p-GaN layers.

3.5 Comparison and Trends

A comparison of the breakdown voltages for both charge imbalance studies is shown in Figure 3.7. Based on this study, a GaN superjunction would have a breakdown voltage that is less sensitive to imbalances in the n-GaN (N_D) layer. The p-GaN layer appears to be extremely sensitive to charge imbalance if the amount of charge exceeds what is ideal for the given geometry.

Both studies of charge imbalance suggest that a superjunction with the n-GaN layer doped higher than the p-GaN layers results in an increase in V_{BR}. This could be benefitial when considering the difficulty of achieving high doping concentrations of p-GaN. This study has considered optimum charge, charge imbalance in the p-type and n-type layers as well as dopant diffusion. Manufactured diodes will experience an increase in total resistance due to a contact resistance between a metal and semiconductor at the P+ and N+ GaN regions. A contact resistance to the P+

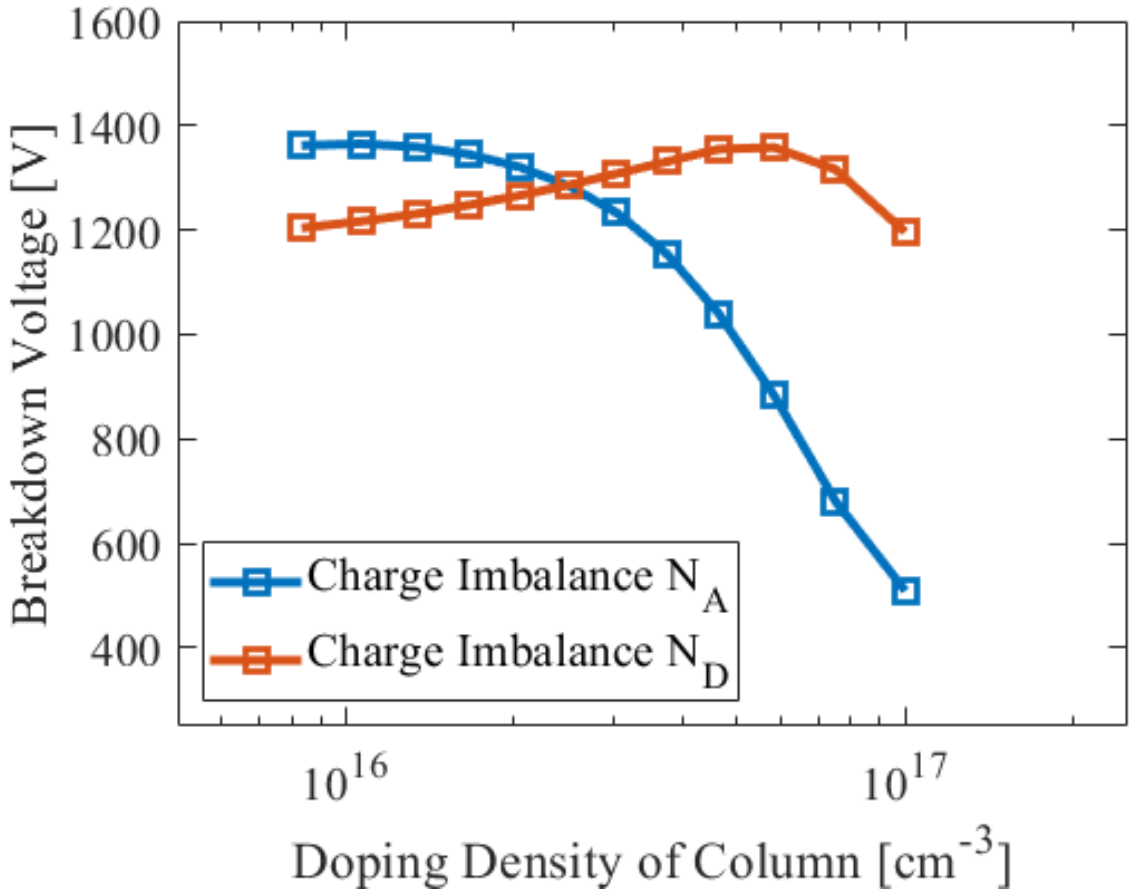

Figure 3.7: Comparison of all charge-imbalanced devices simulated with the red squares representing devices with a N_D charge imbalance and the blue squares representing devices with a N_A charge imbalance.

GaN was set at R_P = 1.0x10^{-4} Ω cm^2 and for N+ GaN R_N = 1.0x10^{-6} Ω cm^2. Both of these values are commonly reported in literature. A summary of breakdown voltage and on-state resistance for all devices studied is shown in Figure 3.8.

The diffused dopant profile impact on device performance was observed to be minimal. The p-GaN metal-semiconductor contact resistance was found to be the most important parameter to realize GaN superjunctions that exceed the uni-polar limit of the material. The inset in Figure 3.7 highlights the majority of the device simulation results and how insignificant each of the non-ideal parameters (dopant diffusion, charge imbalance) had on device performance. This study suggests that GaN superjunctions with charge imbalance and realistic contact resistance could operate at

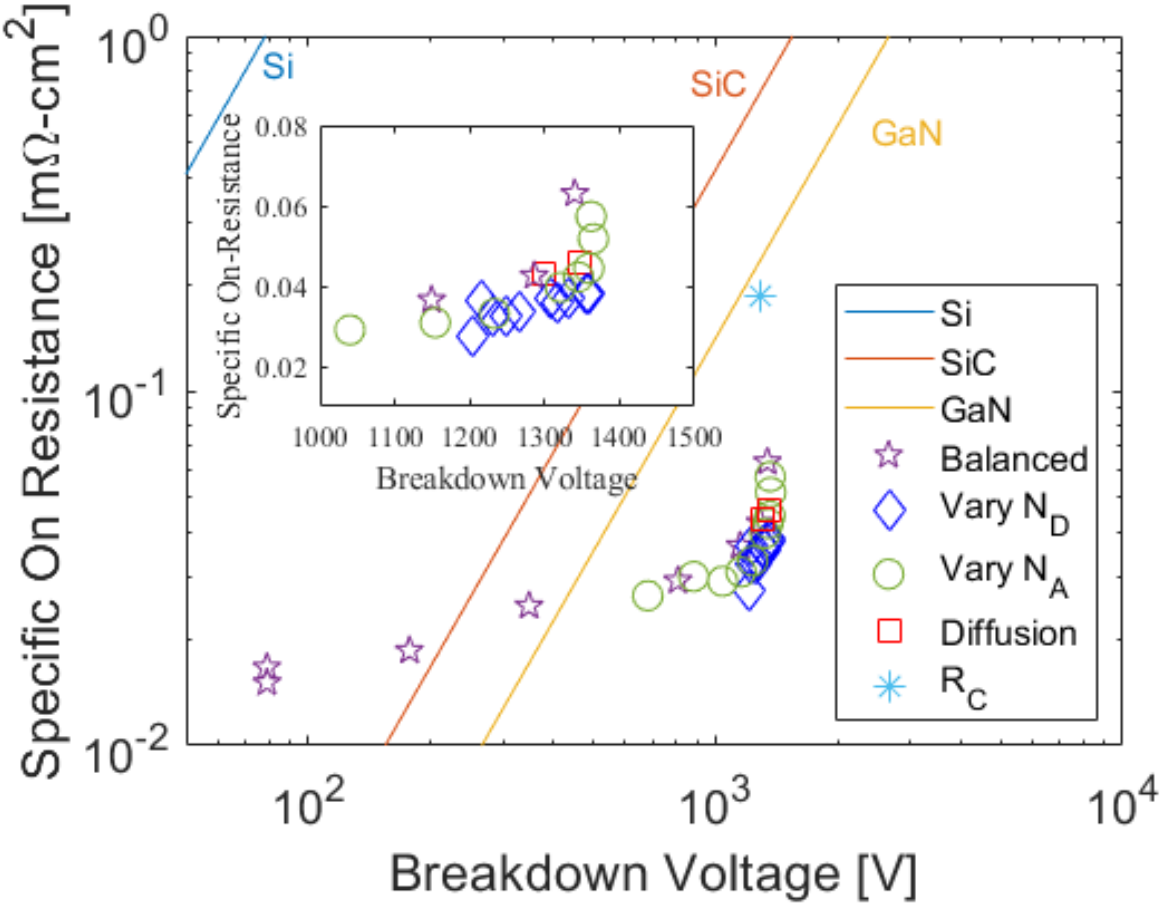

Figure 3.8: Baliga Figure of Merit for all superjunction devices studied. The contact resistance impact R_C has the greatest impact on the device performance for specific on-resistance.

the theoretical limit of GaN. This study concludes that charge imbalance for GaN superjunctions appears to be beneficial in some cases, while dopant diffusion from growth or anneals seems to have a minimal impact on device performance. However, it is clear that a major factor to realizing a GaN superjunctions is achieving low contact resistance to the p-GaN.

4. GALLIUM NITRIDE ON SILICON WITH AN ALD Al_2O_3 BUFFER LAYER

Development of a baseline MOCVD GaN-on-Sapphire (0001) process using Trimethylgallium (TMGa) and Ammonia (NH_3) as precursors is presented in this section with the goals of achieving less than 500 arc-seconds for the FWHM of the GaN (0002) peak using X-ray Diffraction (XRD) and a Root-Mean-Square (RMS) surface roughness of less than 1 nm over a 1 μm^2 area measured by Atomic Force Microscopy (AFM). After these goals are met, the same epitaxial GaN process is applied to Si (100) and (111) substrates that have thin layers of Aluminum Oxide (Al_2O_3) deposited by Atomic Layer Deposition (ALD). The goal of this study is to compare how the GaN grows on the Si (111) and (100) substrates with an ALD Al_2O_3 buffer layer to gain a better understanding of how GaN can be eventually applied to Silicon (100) substrates. This knowledge is applicable to enabling the heterogeneous integration of GaN and Si electronics on the same die.

4.1 Baseline GaN-on-Sapphire Process Development

Amano et. al. reported on the utilization of a low-temperature buffer layer to produce high quality of GaN-on-Sapphire [33] by improving the transition between the substrate and GaN epitaxial layer which have a large lattice mismatch (46 %). Since then, the standard growth procedure for GaN-on-Sapphire consists of a high temperature ramp under H_2, nitridation of the Sapphire surface with NH_3, and a low-temperature buffer layer followed by a high-temperature deposition of epitaxial GaN. The nuclei size and density of the low-temperature buffer layer has a significant impact on the quality of the high-temperature epitaxial GaN layer used for electronic and optical devices [34] [35] [36]. Therefore, development of the GaN-on-Sapphire process began by modifying the low temperature GaN (LT-GaN) growth times to control the thickness of the LT-GaN buffer layer before the high temperature GaN (HT-GaN) film was grown. Sapphire (0001) substrates were cleaned with solvents before being loaded into the MOCVD system. The growth process consists of ramping the chamber pressure to 15 Torr while ramping the 1,000 °C in 10 minutes under an H_2 ambient, followed by a 5 minute H_2 clean and 5 minute nitridation with 5 SLM of NH_3. After

nitridation, the temperature reduced to 525 °C and allowed to stabilize for 1 minute before TMGa was introduced into the process chamber to initiate the LT-GaN growth. After the LT-GaN growth, the TMGa flow was diverted from the process chamber to vent and the temperature was increased to 1,000 °C. The chamber temperature was allowed to stabilize for 1 minute before re-introducing TMGa into the process chamber to grow a HT-GaN film for 30 minutes. A complete list of the process parameters used in this study are show in Table 4.1. Four different LT-GaN growth times were investigated (1 minute, 3 minutes, 5 minutes and 10 minutes) to determine which time gave the best film quality as determined by the FWHM of the GaN (0002) peak using XRD.

Process Parameter	Value
Pressure	15 Torr
Susceptor spin speed	600 rpm
LT-GaN Temperature	525 °C
HT-GaN Temperature	1,000 °C
Nitridation Flows	5 SLM NH_3 + 8 SLM H_2
TMGa Flow Rate	20 sccm
TMGa Vent Pressure	600 Torr
LT-GaN V/III Ratio	1,070
HT-GaN V/III Ratio	3,500

Table 4.1: MOCVD process parameters used in the LT-GaN study for GaN/sapphire.

After growth, the samples were analyzed using a PANalytical Empyrean 2 XRD consisting of a Hybrid monochromator 2xGe(220) for Cu, a fixed 1/2 °divergence slit, a fixed 1mm receiving slit and a 0.10 mm Cu beam attentuator. The ω-rocking curves for the four samples are shown in Figure 4.1. The (0002) peak FWHM for the 1 minute, 3 minutes, 5 minutes and 10 minutes samples were 309 arc-seconds, 1392 arc-seconds, 1555 arc-seconds and 2442 arc-seconds respectively. Broadening of the rocking curve can be attributed to many factors including dislocations, wafer curvature and mosaicity which is the mis-orientation of different crystal grains [37]. The dislocation density of the films can be estimated using the Hirsch model [38]:

$$\rho_{screw} = \frac{\beta^2_{0002}}{9b^2_{screw}} \tag{4.1}$$

$$\rho_{edge} = \frac{\beta^2_{10-12}}{9b^2_{edge}} \tag{4.2}$$

$$\rho_{total} = \rho_{screw} + \rho_{edge} \tag{4.3}$$

where ρ_{screw} and ρ_{edge} is the screw and edge dislocation density in cm^{-2}, β is the broadening of the ω-rocking curve in radians for the (0002) and (10-12) planes respectively and b is the Burgers vector of the dislocation in cm. The magnitude of the Burgers vector for different types of dislocations can be found in literature [39].

The Burgers vector for screw threading dislocations (b_c = <0001>) is calculated to have a magnitude of b_c = 0.5185 nm, which results in a screw dislocation density of 9.27x10^7 cm^{-2} for the 1-minute LT-GaN sample for an associated FWHM of 309 arc-seconds. The estimated screw-type threading dislocation densities for the 3 minute, 5 minute and 10 minute LT-GaN samples were 1.88x10^9 cm^{-2}, 2.34x10^9 cm^{-2} and 5.79x10^9 cm^{-2} respectively. As the ω-rocking curve for the (10-12) plane was not measured, it is not possible to estimate the edge dislocation density. Typically, edge dislocations are the dominate dislocation type in GaN films with densities in the range of 10^8 - 10^{10} cm^{-2} [40], which would result in a total dislocation density, ρ_{total}, in a similar range. Reduction of the LT-GaN times below 1 minute could result in a non-uniform LT-GaN buffer layer. Furthermore, the complete removal of the LT-GaN from the process results in GaN with non-preferential c-plane growth, as confirmed with XRD measurements. The surface of the four samples were analyzed using a Bruker Dimension Icon AFM in Intermittent (Tapping) Mode. Scans of 1μm x 1μm are shown in Figure 4.2.

The measured surface roughness for the 1 minute, 3 minute, 5 minute and 10 minute LT-GaN samples were 0.38 nm, 1.20 nm, 2.24 nm, and 10.2 nm respectively. The surface morphology of the 1 minute and 3 minutes LT-GaN AFM scans is smooth but the termination of threading dislocations

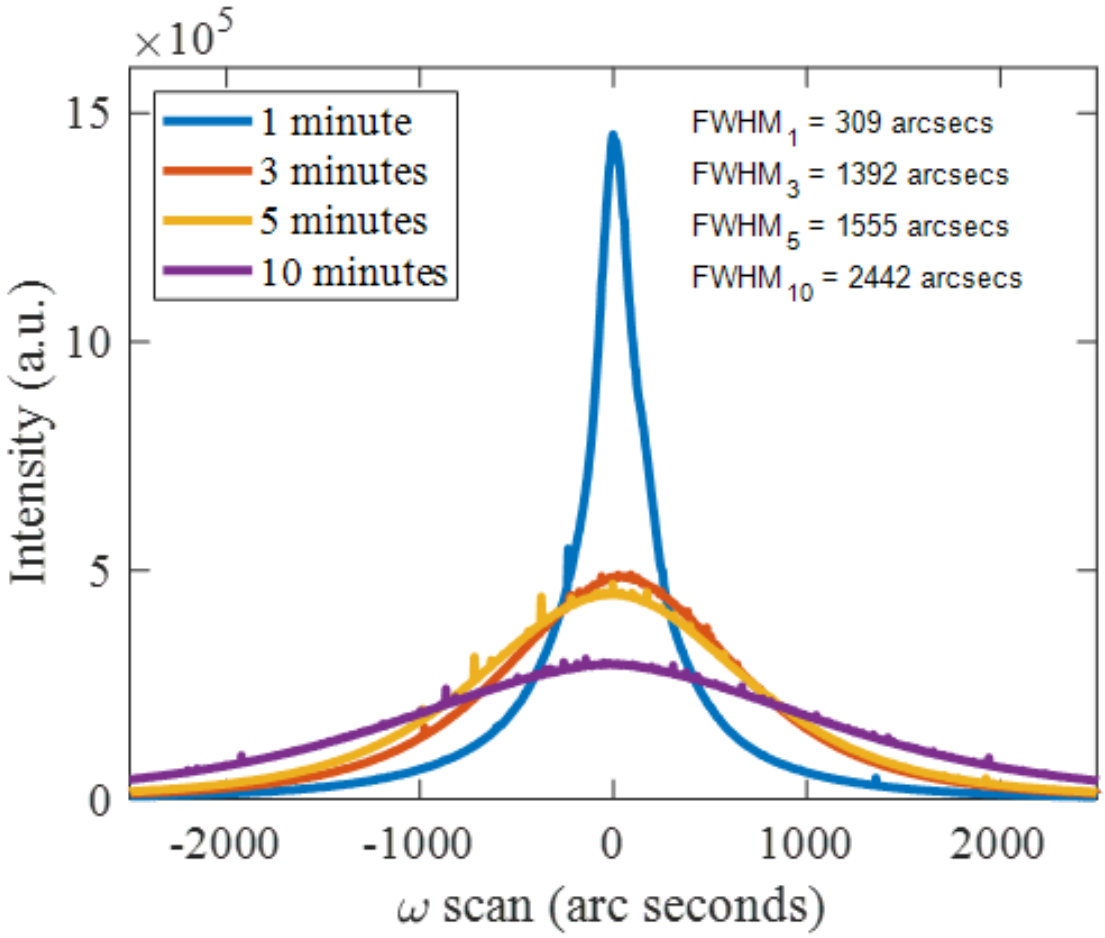

Figure 4.1: XRD rocking curves for the GaN (002) peak on sapphire substrates for different Low Temperature (LT) GaN deposition times.

is apparent at the top surface of the film. As the LT-GaN time is increased, the surface roughness increased and the observation of threading dislocation termination is masked by hillock-like surface morphology. These surface topologies are associated with thicker LT-GaN films that result in subsequently grown HT-GaN films to be more defective. Longer LT-GaN deposition times, or equivalently thicker LT-GaN films, create larger and/or more dense nuclei that will coalesce upon ramping the reactor temperature for the HT-GaN deposition [41]. A preferred size and density of nuclei will lead to higher quality GaN films [42]. The twisting and tilting of the LT-GaN nuclei allows the subsequently grown HT-GaN to grow independently from the substrate surface arrangement. The 1 minute LT-GaN process produced HT-GaN films with the lowest screw-type threading

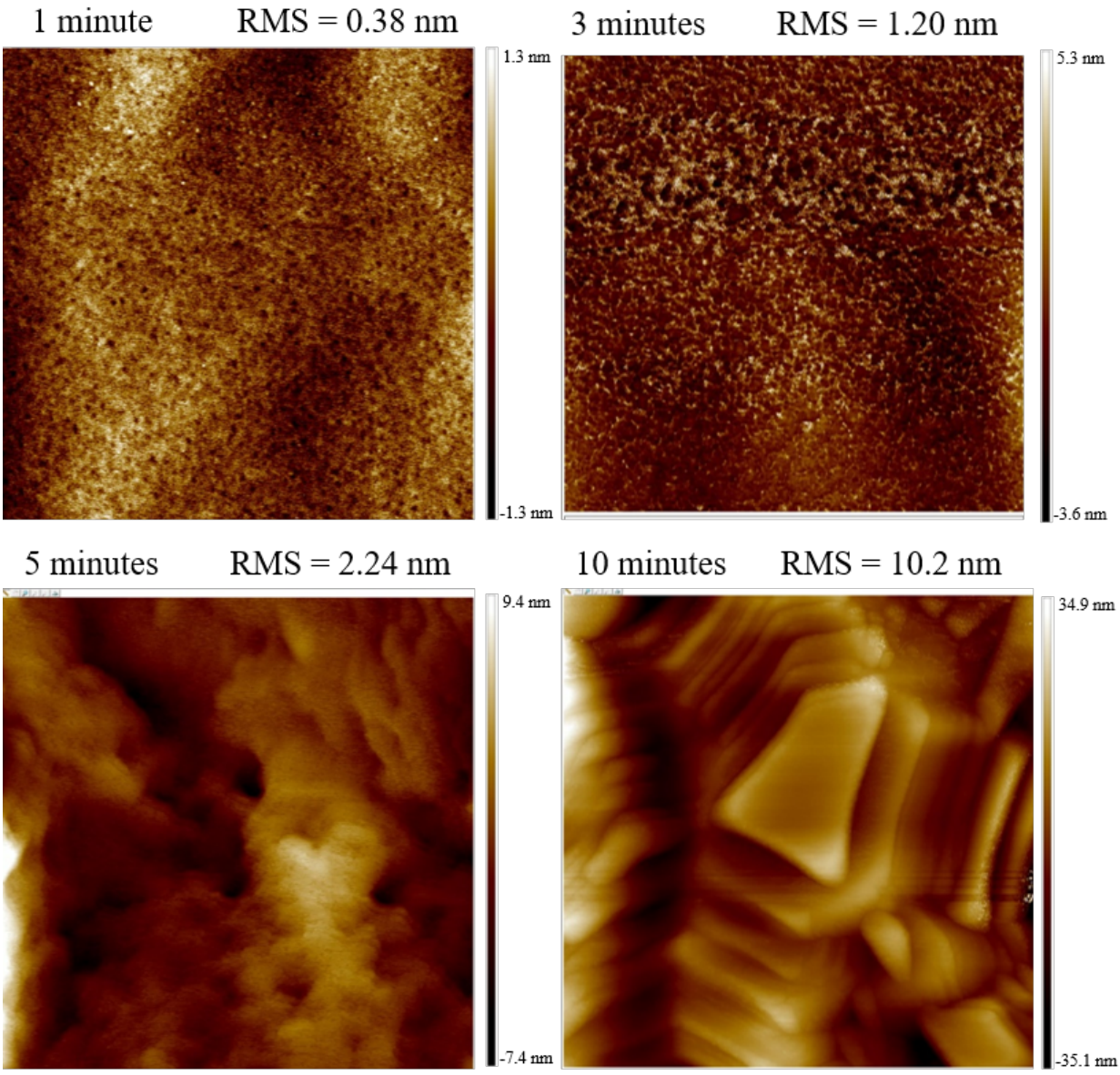

Figure 4.2: 1μm x 1μm AFM scans of the GaN/Al_2O_3 surface for the different LT-GaN growth times.

dislocations, as estimated using XRD, and the smoothest surface as confirmed with AFM. Therefore, this MOCVD process was used to study the utilization of an ALD Al_2O_3 buffer layer on Si (111) and (100) substrates to grow LT and HT-GaN films in the following section.

4.2 GaN-on-Si (111) and (100) with an ALD Al_2O_3 Buffer Layer

The inclusion of an ALD Al_2O_3 buffer layer on Si (111) has been shown to improve the structural and optical quality of the epitaxial GaN by reducing cracking and screw dislocation density [43]. Similarly, the ALD Al_2O_3 buffer layer has been applied to a Si (100) substrate to allow for c-plane GaN to be grown preferentially [44]. Si CMOS is fabricated on Si (100) substrates, while commercial GaN devices are grown on Si (111) substrates. Heterogeneous integration of Si and GaN devices offers the combination of Si circuit complexity and the power electronic benefits of GaN. However, this is typically accomplished with growth of the GaN devices on Si (111), removal of the Si (111) substrate and subsequent bonding of the GaN epitaxial layers to the Si (100) substrate [45]. This process is complex, expensive and difficult to scale. Therefore, the ability to grow GaN directly on Si (100) with appropriate material quality would be a significant breakthrough towards heterogeneous integration. This study aims to understand how GaN grows on Si (111) and Si (100) substrates coated with thin layers of Al_2O_3 deposited by ALD.

4.2.1 ALD Process Development

The process development of ALD Al_2O_3 was performed using a Cambridge Nanotech Savannah 100 ALD system with Trimethylaluminum (TMA) and H_2O as the precursors for Aluminum and Oxygen respectively. The ALD process parameters and associated values are listed in Table 4.2. Silicon (100) and (111) substrates were loaded into the ALD system after degreasing with solvents and a 5 minute Buffered Oxide Etch (BOE) clean to remove any native oxide.

Process Parameter	Value
Temperature	250 °C
Pressure	400 mTorr
H_2O Pulse Time	15 milliseconds
N_2 Purge Time	5 seconds
TMA Pulse Time	15 milliseconds

Table 4.2: Process parameters for deposition of ALD Al_2O_3.

Total cycles were varied to determine a deposition rate using an Ocean Optics NanoCalc DUV Spectroscope to verify the thickness of the ALD Al_2O_3. The measured film thickness versus number of deposition cycles is shown in Figure 4.3.

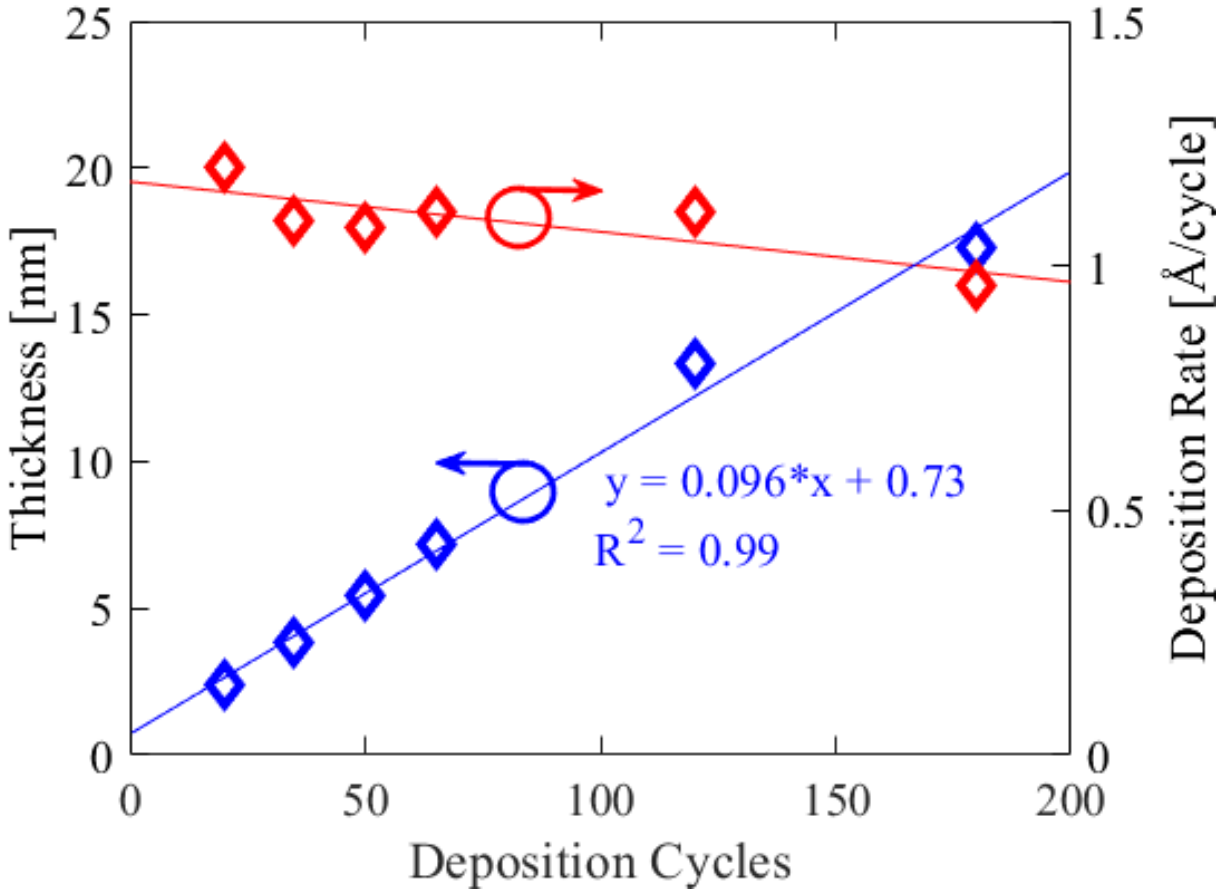

Figure 4.3: Thickness of ALD Al_2O_3 deposited on Si (100) substrate to charaterize the deposition rate and total thickness.

A deposition rate of 0.96 Å was extracted from the deposition cycle versus thickness plot. Therefore, an accurate deposition thickness can be accomplished for the study of ALD Al_2O_3 as a buffer layer on Silicon (100) and Silicon (111) substrates. Silicon (100) and (111) substrates were cleaned using piranha and BOE before the deposition of the ALD dielectric. The piranha is used to remove organic contaminates from the wafer surface and results in a thin amorphous SiO_x layer

on the surface. The subsequent BOE clean removes this oxide and leaves a hydrogen-terminated surface. After the surface clean, the Silicon (100) and (111) wafers were loaded in to the Savannah ALD system. The thicknesses investigated were 3 nm, 5 nm, 7 nm and 10 nm of ALD Al_2O_3 on Silicon (100) and (111) substrates to serve as a nucleation/buffer layer for the LT and HT-GaN layers grown by MOCVD.

4.2.2 Epitaxy and XRD Analysis

GaN deposition on Si (100) and Si (111) substrates with varying thicknesses of ALD Al_2O_3 was performed with the same process outlined in Table 4.1 with a LT-GaN deposition time of 1 minute. After deposition, the GaN films were studied using a Panalytical Empyrean 2 X-ray Diffraction instrument (XRD) as shown in Figure 4.4.

The $2\theta-\omega$ scans for the 5nm ALD Al_2O_3 on Silicon (100) and (111) substrates are compared to the GaN/Al_2O_3 from the previous section. A long range scan is performed to include measurements of the (0002), (0004) and (0006) film peaks of the GaN to allow for more in-depth analysis, as will be discussed later. The 5nm ALD Al_2O_3 on Silicon (100) and (111) signals are amplified post-measurement by 10,000x and 100x to enable easier comparison. In the $2\theta - \omega$ range of 20°to 45°a background amorphous signal is present, which is attributed to the LT-GaN. Based on the $2\theta - \omega$ scans, each peak location and integral breadth for the GaN (0002), (0004) and (0006) planes can be determined and the lattice parameter, c, using Bragg's Law and the equation for spacing between hexagonal crystal planes,

$$n\lambda = 2dsin(\theta) \tag{4.4}$$

$$d = \sqrt{\frac{1}{(h^2 + k^2 + hk)\frac{4}{3a^2} + \frac{l^2}{c^2}}} \tag{4.5}$$

where n an integer, λ is the wavelength of $K_{\alpha-1}$ wavelength of Cu X-rays (1.540598 Å) , d is the spacing between crystal planes, θ is the angle at which the XRD peak is observed, with (hkl) representing the crystal plane of interest and with a $\&$ c representing lattice parameters of the

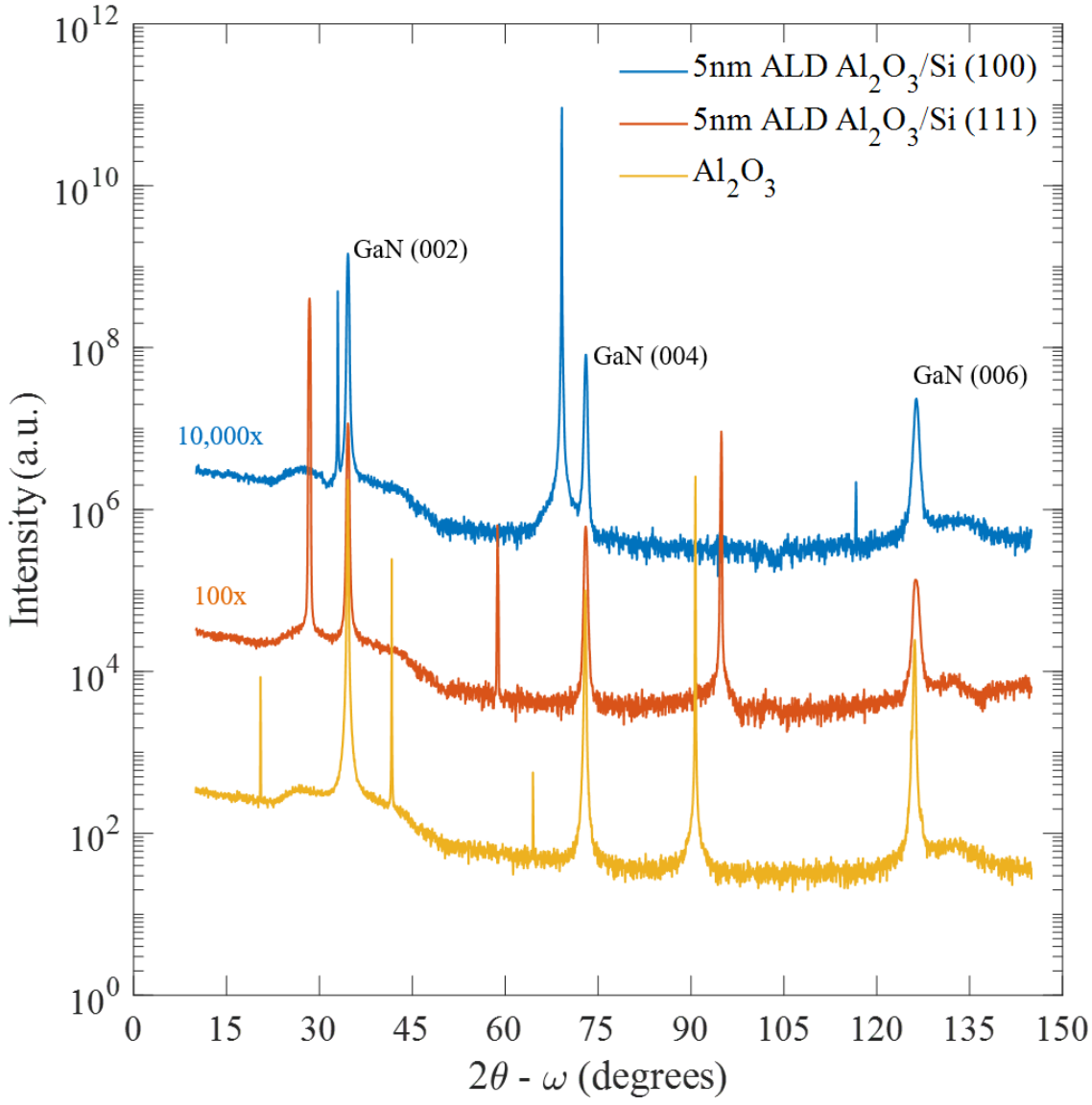

Figure 4.4: XRD $2\theta - \omega$ scans of the GaN grown on sapphire, Si(100) and Si(111) that also had 5nm of ALD Al_2O_3. The Silicon (111) and Silicon (100) intensities have been scaled by 100x and 10,000x to allow for comparison.

hexagonal crystal structure. The notation for (hkl) to (hkil) for hexagonal crystal structures is that i = -(h+k). Error in sin(θ) at low θ angles can lead to improper calculation of the lattice parameter, therefore the higher order peak locations, (0004) and (0006), are used to precisely extract the c-lattice parameter for GaN [37]. The calculationg of the strain perpendicular to the c-plane for the

GaN on Silicon films is shown in Figure 4.5. An average of the two higher order peaks is used to determine the lattice parameter c for the 3 nm and 5 nm films, with the error bars representing one standard deviation. For the 7 nm and 10 nm films, only the (0004) peak was used to calculate the lattice parameter and the error bars represent the standard deviation of the (0002) and (0004) peak locations. A summary of all c lattice parameters extracted from the grown GaN films is shown in Table 4.3

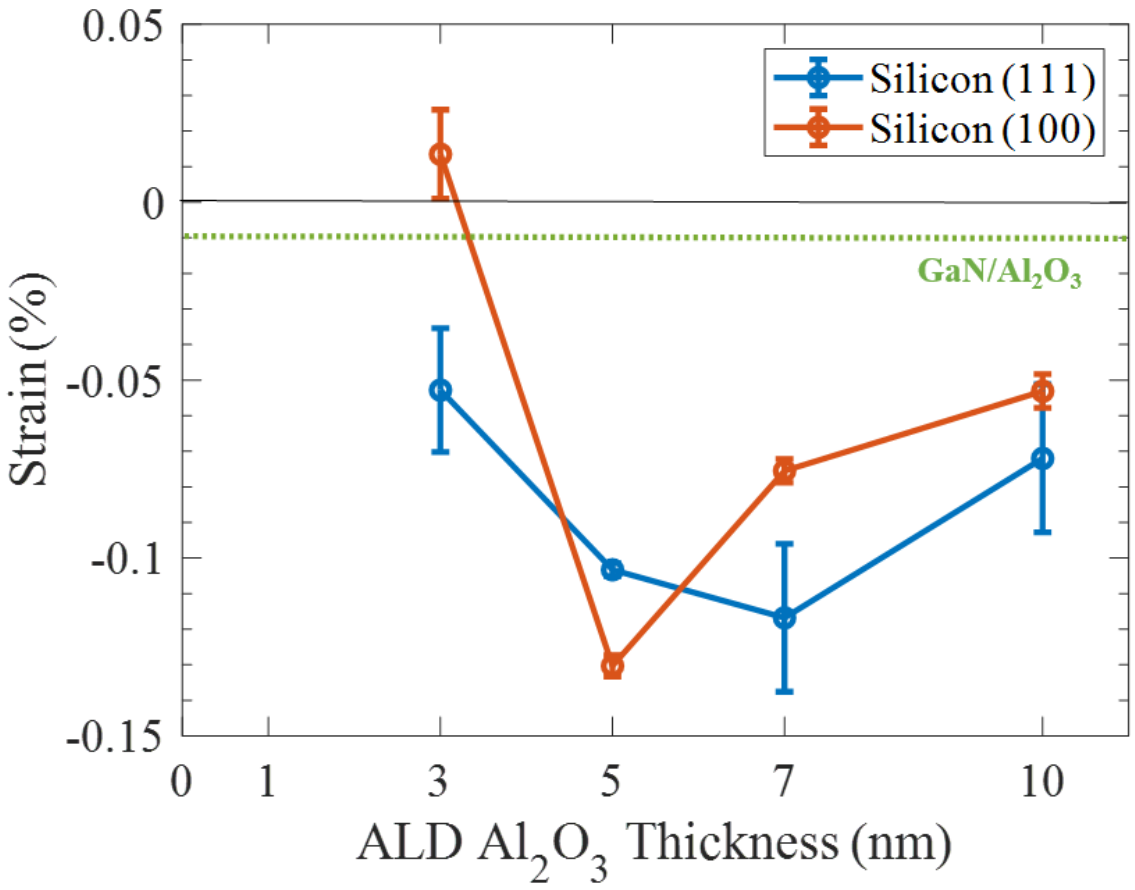

Figure 4.5: Strain calculations based on lattice parameters estimated from (0004) and (0006) XRD peaks. The dotted line represents the strain calculation for the GaN-on-Al_2O_3 with 1 minute LT-GaN.

The 3 nm GaN on Silicon (100) film has error bars large enough to suggest that the film has

relaxed. As the thickness of the ALD Al_2O_3 is increased, the strain reaches a maximum at 5 nm and reduces as the ALD film thickness increases. For the GaN on Silicon (111) films, the strain increases until a maximum is reached at 7 nm and reduces for the thicker ALD film.

Ideal GaN c-plane spacing	5.1851 Å
GaN/Al_2O_3	5.1843 Å
ALD Al_2O_3 on Silicon (100)	GaN c-plane spacing (Å)
3 nm	5.1823
5 nm	5.1797
7 nm	5.1811
10 nm	5.1823
ALD Al_2O_3 on Silicon (111)	GaN c-plane spacing (Å)
3 nm	5.1858
5 nm	5.1783
7 nm	5.1790
10 nm	5.1813

Table 4.3: Summary of c-plane spacing of the GaN films grown on ALD Al_2O_3 with varying thicknesses on Si (100) and (111) substrates.

As mentioned previously, the FWHM of the GaN (0002) is a metric used to understand the quality of the film, with a smaller FWHM value corresponding to a film with a better crystal structure. All the FWHMs of the GaN films is shown in Figure 4.6. The GaN films with the lowest FWHM were 5 nm of ALD Al_2O_3 for both the Silicon (100) and (111) substrates. These results agree with the findings of [43] in that 5 nm of ALD Al_2O_3 buffer layer produced the highest quality GaN film. Interestingly, the GaN-on-Si (100) films track the quality of the GaN-on-Si (111) films for the thicknesses investigated. To improve the quality of the epitaxial GaN, thicker ALD layers (20 nm and 35 nm), longer LT-GaN deposition and nitridation times, and a high temperature (1,200 °C) anneal of the ALD Al_2O_3 in an inert and O_2 ambient were studied. However, all films had poor surface morphology and crystal quality except the 5 nm ALD films on both substrates.

Two contributors to peak broadening in XRD are finite crystallite size and strain in the thin film under measurement. Furthermore, instrumental effects play a role in peak broadening by imperfect

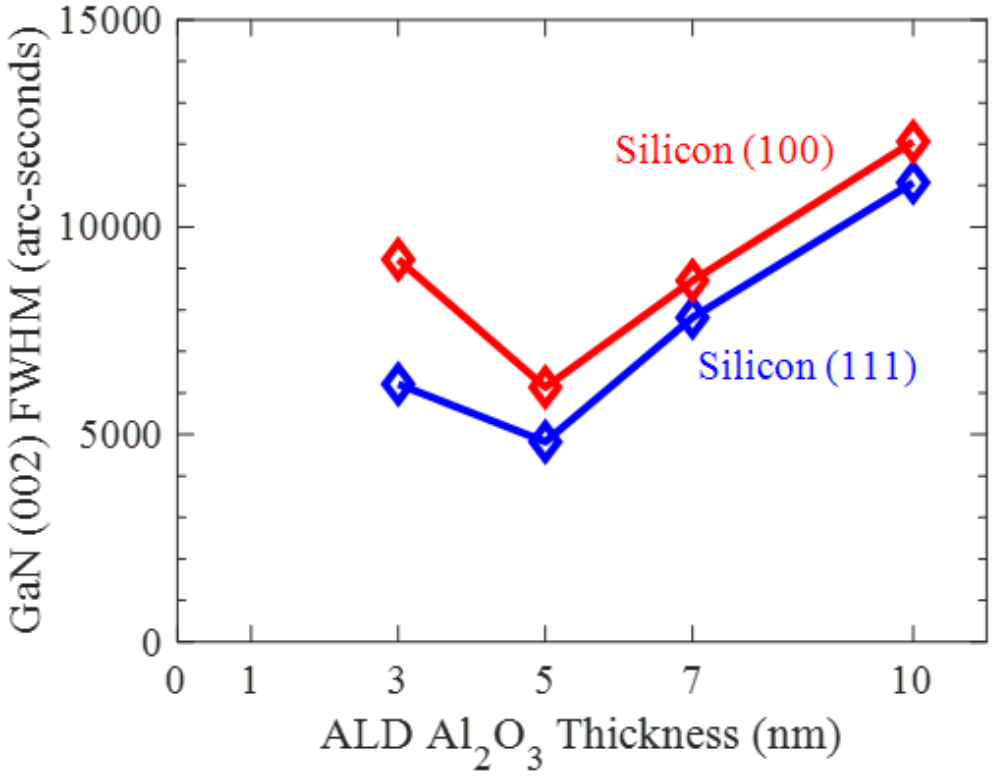

Figure 4.6: A comparison of the FWHM GaN (002) peak for the Silicon substrates with varying thicknesses of ALD Al_2O_3.

focusing and finite widths of the Cu X-ray peaks [37]. Determination of the crystallite size and strain is possible by using a Williamson-Hall plot (WH) [46]. Diffraction peaks obtained from ω scans can be Gaussian, Lorentzian or a combination of both. This becomes important when subtracting out the peak broadening due to instrumental effects. However, the peak broadening due to instrument effects are considered negligible for the GaN-on-Silicon samples due to the large FWHM (> 1,000 arc-seconds) of the (0002) peaks. The expression for peak broadening due to small crystallite size was derived by Scherrer as:

$$B_{crystallite} = \frac{k\lambda}{Lcos(\theta)} \tag{4.6}$$

where λ is the x-ray wavelength, θ is the Bragg angle, L is the average crystallite size and k is a constant which depends on the crystal structure and profile type. Values in the range of 0.89

to 1.39 have been reported for k, but typically k is taken as unity with an assumed error of $\pm$ 10 $\%$ [37]. The other main source of peak broadening is due to lattice strain, η, in the thin film and follows the equation:

$$B_{strain} = \eta tan(\theta) \tag{4.7}$$

Combining the equations for broadening due to small crystallite sizes and lattice strain and multiplying by cos(θ) the following equation is obtained that allows the extraction of lattice strain and crystallite size from the XRD curves:

$$B_t = B_{crystallite} + B_{strain} \tag{4.8}$$

$$\frac{B_t cos(\theta)}{\lambda} = \frac{k}{L} + \frac{\eta sin(\theta)}{\lambda} \tag{4.9}$$

Therefore, by plotting the above equation, were B_t is the integral breadth of the XRD peak in radians, a straight line should be observed that has a slope of proportional to η and an intercept proportional to the crystallite grain size, L. Full range scans for all films measured was not obtained and the peak broadening due to instrumental effects was not measured. Therefore, a discussion about trends in strain and crystallite size will be made based on the strain calculations. The GaN on Silicon (100) film with 5 nm ALD had the most strain but also had the lowest FWHM, which implies that the grain size is the largest. Similarly, GaN on Silicon (111) film with the 5 nm ALD had the second highest strain, but a significantly lower FWHM than all the other ALD film thicknesses. Therfore this film too should have the largest grain size for the GaN on Silicon (111) films. As the ALD thickness is increased on both substrates, the strain reduces, but the FWHM is increasing, which implies that the grain size is smaller. The GaN films with a 5 nm ALD Al_2O_3 buffer layer on both Si substrates had a mirror like surface, unlike the all the other films deposited. Therefore, only these GaN films with a mirror-like surface were used for electronic device fabrication.

4.2.3 Ohmic and Schottky Contacts

Ohmic contacts and schottky diodes were fabricated from the GaN films with a 5 nm ALD Al_2O_3 buffer layer on both Si substrates. The device fabrication process began with a 5 minute BOE clean followed by a DI rinse. PECVD was then used to deposit 100 nm of Si_3N_4 field dielectric. Dark field contact lithography was performed to open windows in the field dielectric by a 5 minute BOE etch. Before the ohmic metal, Titanium, was evaporated the sample was exposed to a 2 minute 1:1 HCl:DI clean to remove oxides from the GaN surface. The Lesker PVD 75 E-beam evaporator was pumped to a base pressure of 5x10^{-6} Torr before depositing 250 nm of Ti on the samples. Bright field contact lithography was performed on the samples to transfer the pattern to the ohmic contact pads by a 20:10:1 DI:BOE:H_2O_2 Ti etch, which required about 1 minute 30 seconds to complete. Circular TLM was then performed on the sample with the as-deposited Ti ohmic contacts. The inner pad diameter was 120 μm and the spacing between the two pads ranged from 13 - 32 μm. A correction factor was applied to the data to minimize error in the TLM extraction [47] due to the inner pad diameter not being significantly larger than the electrode spacing. The semiconductor sheet resistance, specific contact resistance and transfer length can be found by:

$$R_T = \frac{R_{SH}}{2\pi L}(d + 2L_T)C \tag{4.10}$$

$$C = \frac{L}{d} ln(1 + \frac{d}{L}) \tag{4.11}$$

where R_T is the total measured resistance in Ω, R_{SH} is the semiconductor sheet resistance in Ω-square, L is the inner pad radius, d is the spacing between the inner and outer electrode, L_T is the transfer length and C is the correction factor. The TLM data for the two GaN films with a 5 nm ALD Al_2O_3 buffer layer on Si (100) and Si (111) is shown in Figure 4.7. The sheet resistance of the GaN on Si (100) and Si (111) is calculated to be 5013 Ω-square and 30,318 Ω-square respectively. The transfer length, defined as the distance at which 1/e of the voltage has been dropped across the

contact. The specific contact resistivity, ρ_C is calculated from

$$L_T = \sqrt{\frac{\rho_C}{R_{SH}}}. \tag{4.12}$$

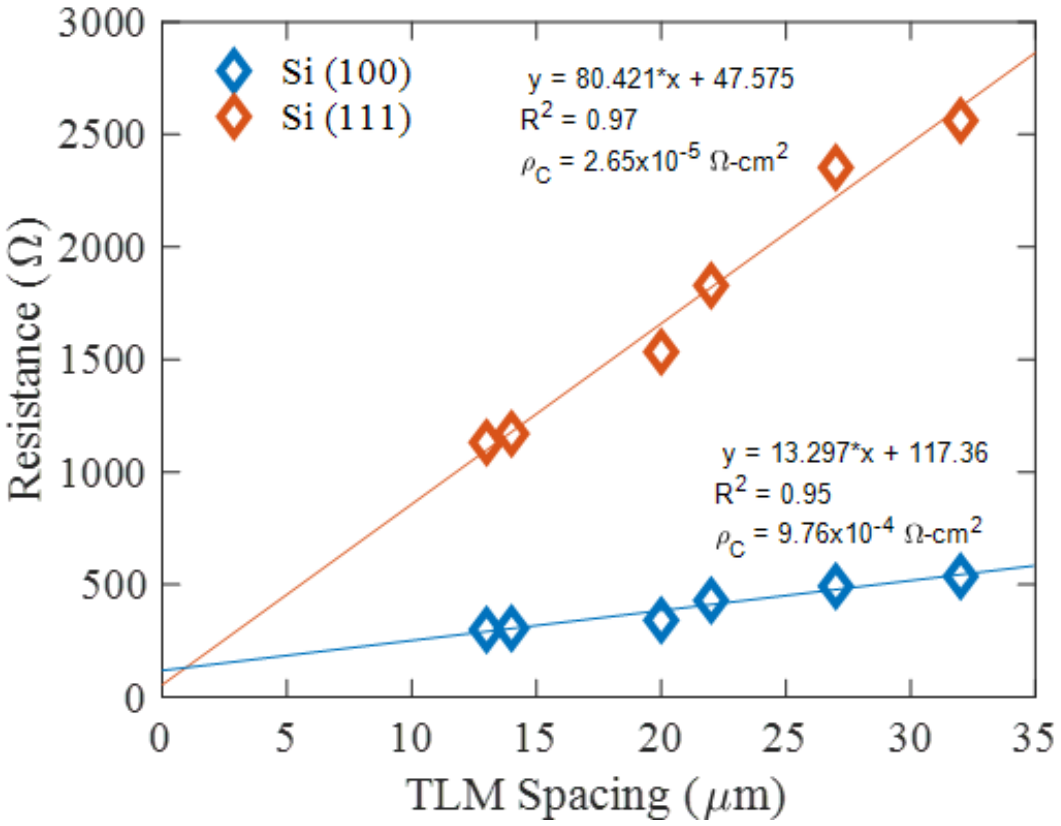

Figure 4.7: TLM plots of the as-deposited Titanium ohmic contacts to the GaN films with a 5 nm ALD Al_2O_3 buffer layer on Si (111) and Si (100).

The lower sheet resistance of the GaN-on-Si (100) can be attributed to a higher background doping concentration or more defects, which is supported by the broader GaN (002) peak. Interestingly, the ρ_C for the GaN-on-Si (100) sample is approximately 40x higher than the GaN-on-Si (111) despite the lower sheet resistance. This is attributed to more defects, potentially surface states and a generally more defective film.

Schottky diodes were then fabricated from the devices with the ohmic contacts already on them. The process continued with a 200 nm Ni evaporation followed by a standard bright field lithography process. The Ni was etched using Ni TFB etchant and the etch time was 7 minutes. After fabrication the diodes looked like that stuff shown in Figure 4.8.

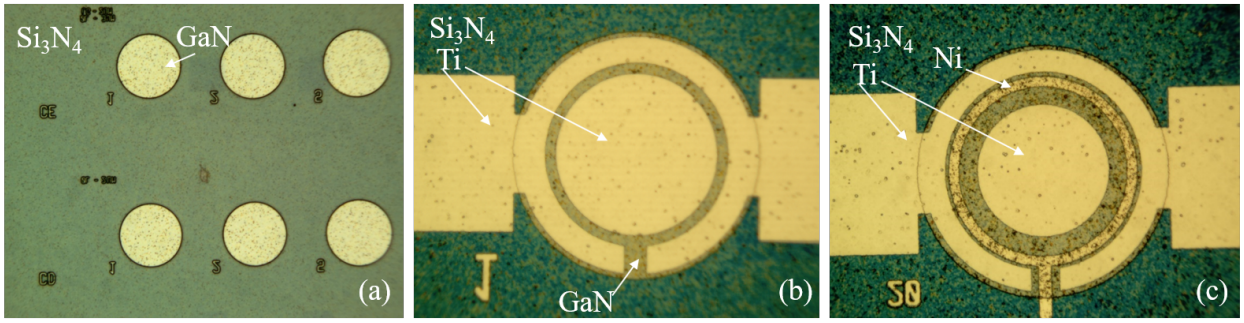

Figure 4.8: Microscope images of the fabrication process of Ni schottky diodes to the GaN on Silicon (111) and (100) substrates. (a) Microscope photo after the first lithography step of etching an active area in the nitride field dielectric (b) Microscope photo after the second lithography step of etching the ohmic contact pads. (c) Microscope photo after the Schottky diode is complete with a patterned Ni Schottky contact.

After fabrication the diodes were analyzed using the HP4155B parametric analyzer. The I-V sweeps of two of the diodes made from the Si (111) and Si (100) substrates with 5 nm of ALD Al_2O_3 are shown in Figure 4.9. Look at these curves and see how the Si (100) sample conducts less current in forward and reverse bias and the Si (111) diode conducts more current. Forward and reverse bias characteristics can be extracted to get you some barrier height, ϕ_B, the reverse saturation current, J_0, and the ideality factor, n.

Furthermore, the doping density, N_D can be extracted from the reverse bias conditions based [48]. The current density, J, expression for a metal-semiconductor with a forward bias is

$$J = J_0 exp(\frac{qV}{nk_BT}) \tag{4.13}$$

where J_0 is the reverse saturation current, q is the electron charge, V is the applied voltage, n is

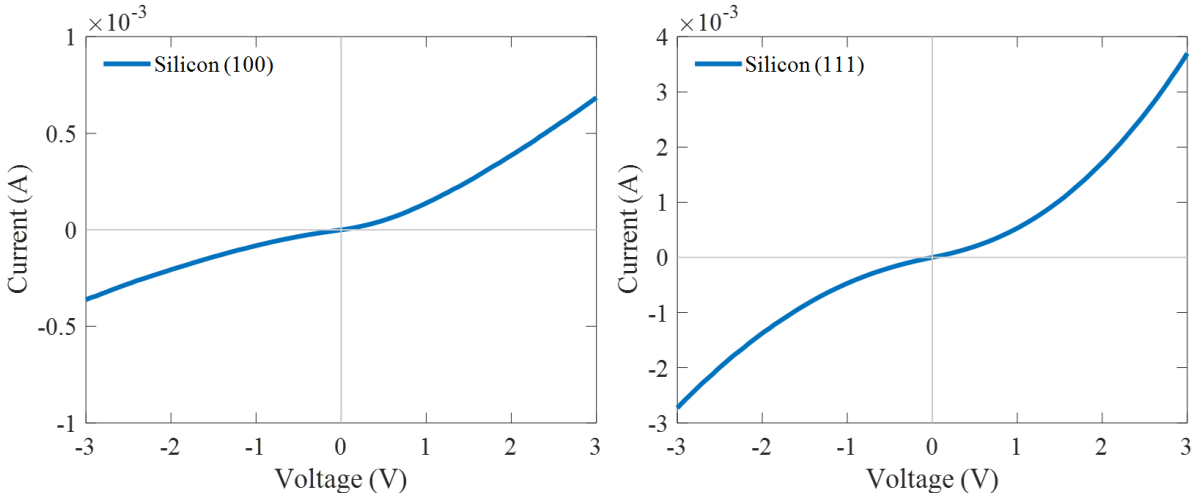

Figure 4.9: (a) I-V plot of GaN-on-Silicon (100) diodes with 5 nm ALD Al_2O_3 thickness (b) I-V plot of GaN-on-Silicon (111) diodes with 5 nm ALD Al_2O_3 thickness.

the ideality factor, k_B is Boltzmann's constant and T is temperature. The reverse saturation current and ideality factor can be extracted by taking the log the the above expression,

$$ln(J) = ln(J_0) + \frac{qV}{nk_BT} \tag{4.14}$$

Therefore, plotting ln(J) versus the applied bias V the reverse saturation current can be found by extrapolating to V = 0 and the slope of the curve gives the ideality factor, n. The forward and reverse bias curves used for parameter extraction from the GaN grown on 5nm ALD Al_2O_3 on Si (100) and Si (111) substrates are shown in Figure 4.10. It is important to take the linear fit of the ln(J)-V curve at voltages much greater than kT, due to some effects while also making sure to not have the data taken far above 1V due to series resistance. The linear fit is made for the voltages in the range of 0.5 to 1V for the forward bias and -1V to -0.5V for reverse bias.

After the reverse saturation current has been determined, the barrier height can be estimated from,

$$\phi_B = \frac{k_BT}{q} ln(\frac{A^*T^2}{J_0}) \tag{4.15}$$

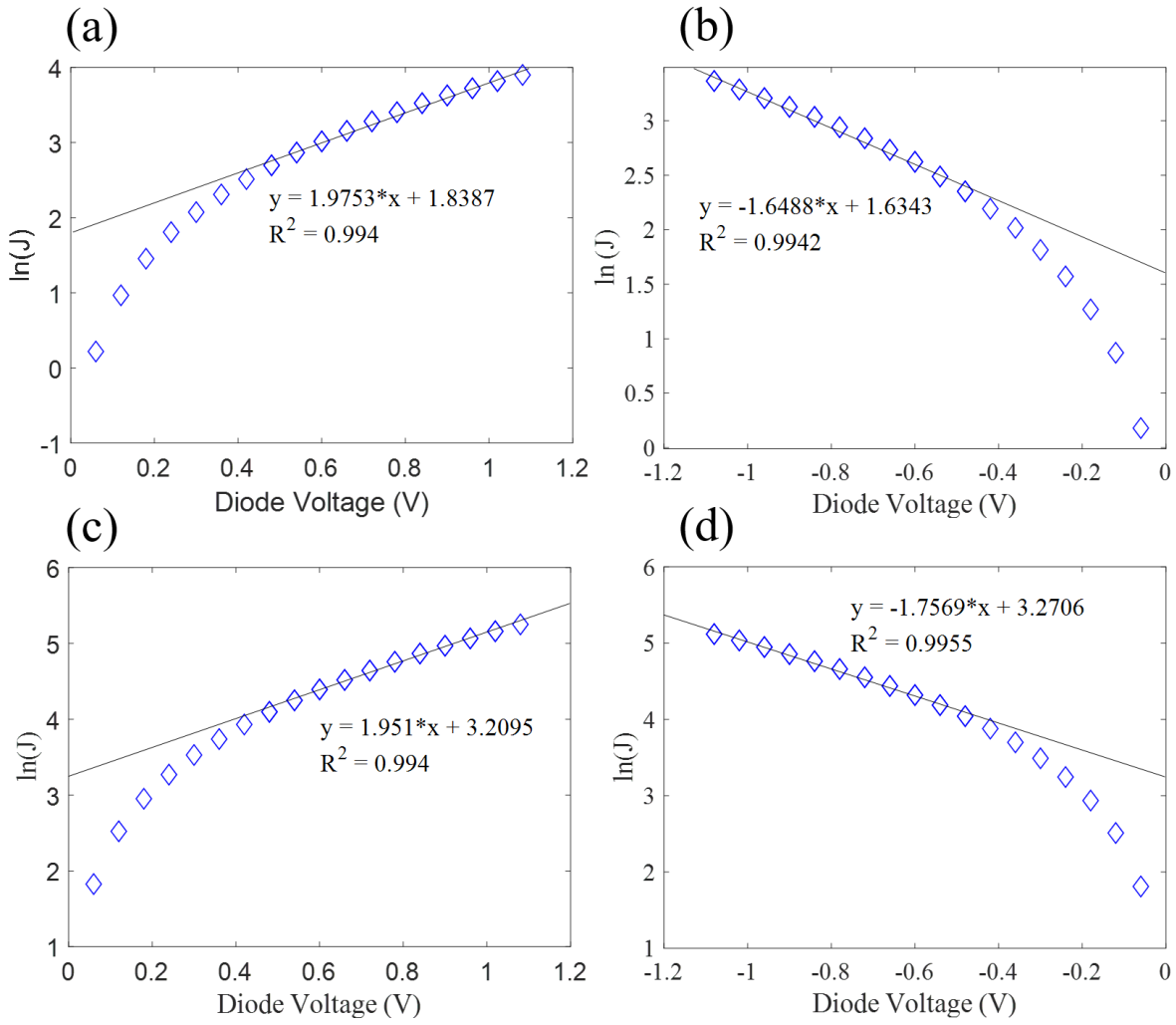

Figure 4.10: Extraction of diode parameters for forward and reverse bias. (a) Silicon (100) forward bias (b) Silicon (100) reverse bias (c) Silicon (111) forward bias (d) Silicon (111) reverse bias.

where ϕ_B, is the barrier height, A* is the modified Richardson constant which was 26.64 units.

A comparison of all the extracted information from these Silicon diodes is shown in Table 4.4.

Substrate	J_0 (A-cm^{-2})	n	ϕ_B (eV)	N_D (cm^{-3})
Silicon (100)	6.28	19.47	0.334	5.17x10^{17}
Silicon (111)	24.7	19.71	0.298	5.53x10^{17}

Table 4.4: Comparison of the extracted diode parameters for the diodes made from Silicon (111) and Si (100).

Differences in reverse saturation currents are observed for the GaN on Silicon films, with the other extracted parameters in Table 4.4 being similar. The poor specific contact resistance to the GaN on Silicon (100) leads to a reduced reverse saturation current but also limits the on-state current. Therefore, an engineering trade-off exists between the two GaN films on different Silicon substrates.

4.2.4 GaN-on-Sapphire Schottky Diodes

Literature shows that cleaning the GaN surface with Hydrochloric acid (HCl) and Buffered Oxide Etch (BOE) leads to a reduction in the oxygen and carbon concentration on the surface, enabling improved contact resistance between a given metal and the semiconductor surface. The ohmic contact process to GaN/sapphire films deposited by MOCVD began with a two-step surface pre-clean of 1:10 HCl:DI-H_2O rinse for 10 minutes followed by 2 minutes of rinse in DI-H_2O and concluded with a 3 minute clean in Buffered Oxide Etch (BOE) followed by a 2 minute rinse in DI-H_2O. After the surface pre-clean, 120nm of Plasma Enhanced Chemical Vapor Deposition (PECVD) Silicon Nitride (Si_3N_4) was deposited as a field dielectric. A lift-off process using contact lithography was then performed on the sample using AZ5214E-IR and LOR-3A photoresist. After soft-bake, exposure, development and hard-bake the Si_3N_4 field dielectric was etching using BOE for 4 minutes followed by a 2 minute rinse in DI-H_2O. Before metal deposition, a 2 minute clean in 1:10 HCl:DI-H_2O was performed followed by a 2 minute rinse in DI-H_2O. The sample was then loaded into a PVD Lesker evaporator where 20nm of Titanium were deposited on the semiconductor surface followed by a 200nm deposition of Aluminum. Once the metal stack was deposited, the PVD system was vented and the sample was placed in AZ400T photoresist stripper for 10 minutes at 120 °C. The final TLM structures are shown in the inset of Figure 4.11. A ρ_C was extracted from the TLM plot to be 2.11x10^{-6} Ω cm^{-2}.

Hall measurements were performed on a similar sample with large Ti/Al contacts deposited with evaporation and a shadow mask. The extracted background electron concentration was determined to be in the range of 0.8x10^{18} cm^{-3} to 2.0x10^{18} cm^{-3} with associated mobilities in the range of 50 to 100 cm^2/Vs. This provides an idea of the background doping concentration present

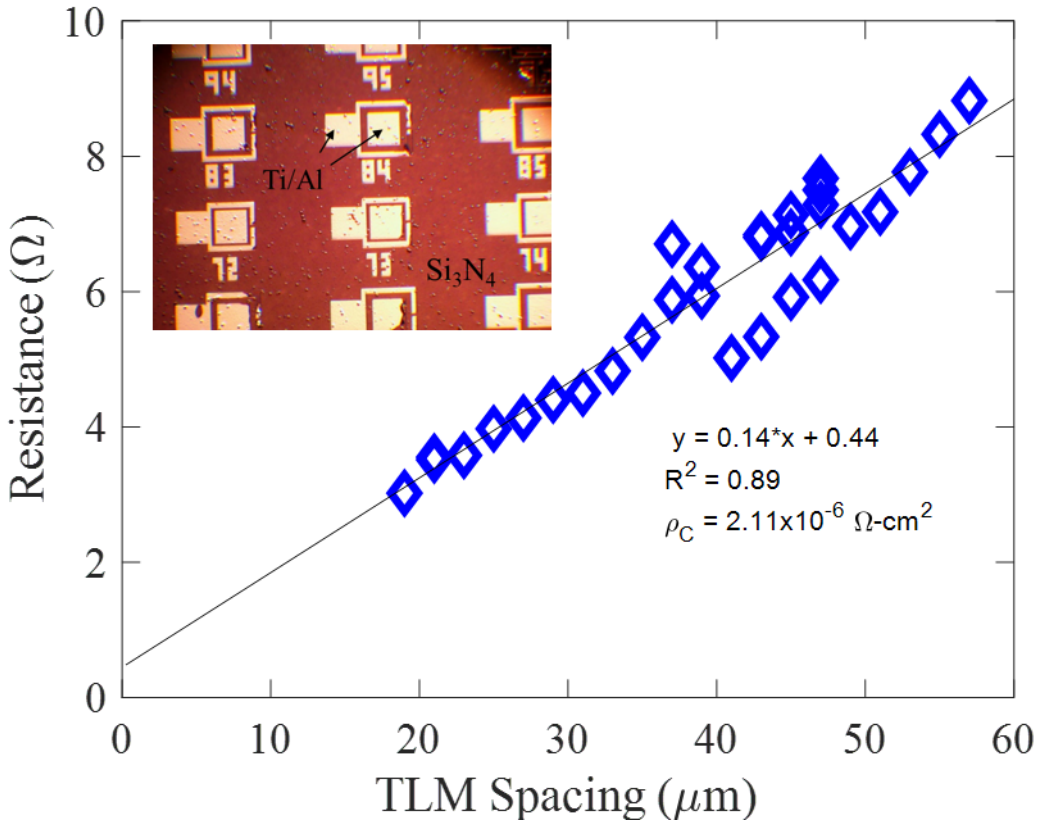

Figure 4.11: TLM plot for Ti/Al contacts to the GaN/sapphire process developed previously.

in the as deposited GaN layer that will be subsequently used as a preferred nucleation site for SAE. A similar ohmic contact process was employed for making ohmic contacts to the SAE GaN in the following discussion.

Ohmic contacts to the SAE GaN structures shown in Figure 5.1(a) began with a 2 minute 1:1 HCl:DI clean. Then the samples were loaded into a DC sputter system for Ti deposition. Sputtering was utilized to ensure proper coverage of metal around the SAE GaN structure due to the non-conformal nature of e-beam evaporation. The sputtering was performed at 7 mTorr for 35 minutes at a sputter power of 450 W. The standard lithography process was then performed with patterning of the Ti being accomplished with an 80 second BOE etch. The photoresist was removed and the sample was anneal in a N_2 ambient for 240 seconds at 575 °C. The annealing process helps improve the ohmic contacts. The results of the TLM process are shown in Figure 4.12.

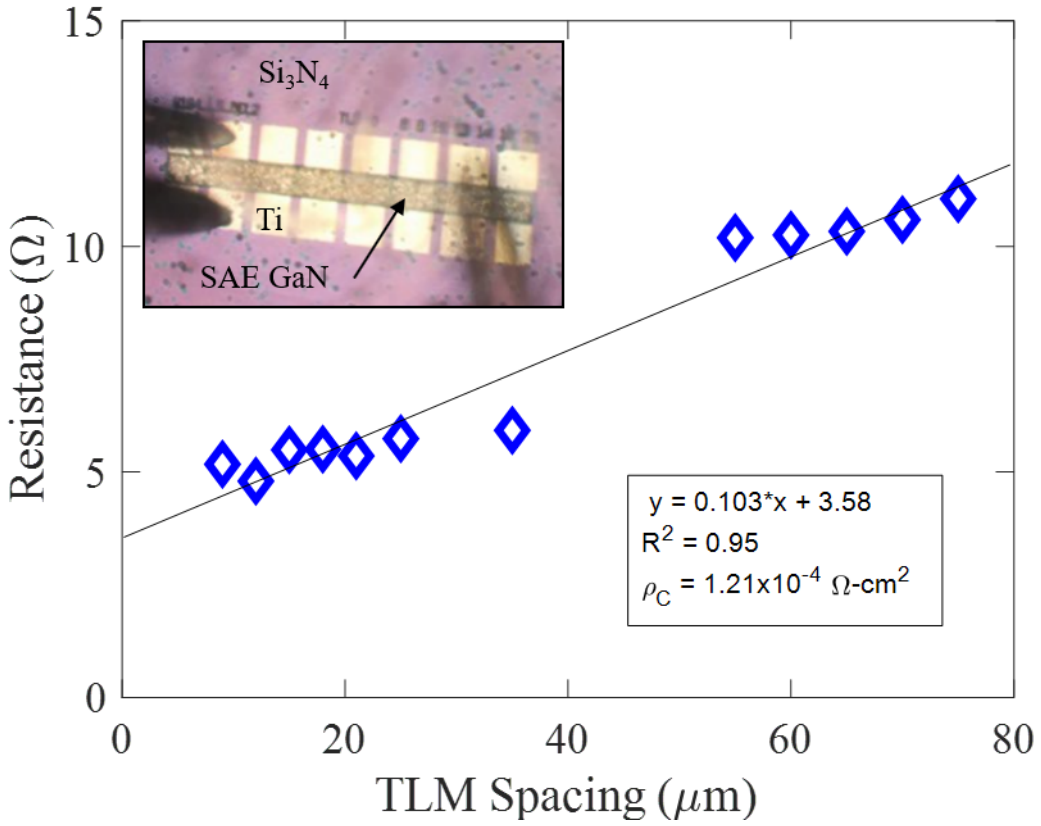

Figure 4.12: TLM plot for sputtered Ti films on the SAE GaN/sapphire.

The schottky contact process began with a 2 minute 1:1 HCl:DI clean followed by the deposition of Cr by DC sputter at 350 W, 7 mTorr for 40 minutes. The Cr schottky metal was patterned by standard lithography and CR-1A etch for approximately 90 seconds. A final anneal in a N_2 ambinet was performed at 350 °for 120 seconds. The electrical results for the schottky GaN device are shown in Figure 4.13. An HP4155B parametric analyzer was used to perform the I-V measurements and a Agilent LCR meter was used to measure the $1/C^2$ data that enabled background doping concentration extraction. You need to talk about the potential differences in GaN sheet resistances between the blanket and SAE GaN.

The schottky diodes produced $1/C^2$ data that suggests the background doping concentration in the SAE GaN is approximately 10^{18} cm^{-3} with an R^2 value of 0.74. This result is similar to that of the hall measurement for the underlying GaN nucleation layer. These results agree with literature

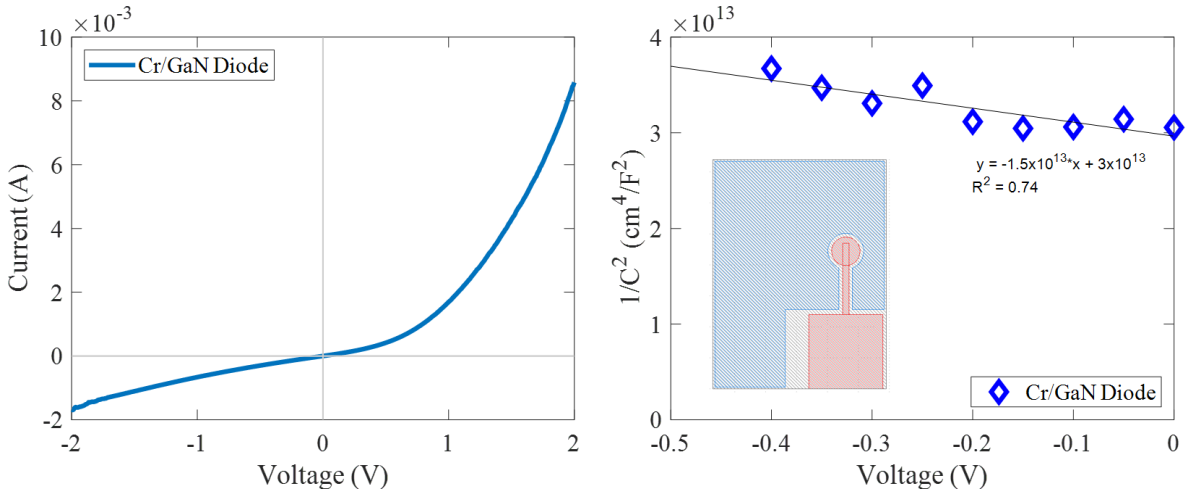

Figure 4.13: (a) I-V curve for Cr/GaN schottky diodes with Ti ohmic contacts. (b) $1/C^2$ plot used to extract the doping density of the unintentionally doped GaN films.

that defects propagate into the overgrown GaN and that other interesting things happen. Now that the background doping concentration of the MOCVD process has been understood and ohmic and schottky diodes have been successfully fabricated, the Aspect Ratio Trapping (ART) process on Si (111) substrates can be developed.

5. SELECTIVE AREA EPITAXY

Currently, a commercially viable native substrate for GaN does not exist which has required researchers to utilizing lattice-mismatched substrates to grow GaN films. This hetero-epitaxy produces GaN films with defect densities in the range of 10^8 - 10^{10} cm^{-2} on Sapphire, SiC and Silicon substrates. Stacking faults and inversion domains can form non-radiate recombination centers which reduce quantum efficiencies and act as scattering centers. Furthermore, impurities will diffuse more readily along threading dislocations which can also impede carrier transport in lateral structures. Defects that are electrically active can cause increased leakage currents that are detrimental to power electronic devices. Selective area epitaxy (SAE) is a technique used to reduce defect densities to values of approximately 10^6 cm^{-2} for GaN films. Laser diodes fabricated from SAE-GaN films experienced an increase in lifetime from 300 hours to over 10,000 hours [49] due to the reduced defect densities. Furthermore, SAE-GaN films have shown a reduction of three orders of magnitude in leakage currents for p-n diodes [50]. These SAE-GaN films are typically grown by first depositing a dielectric (Si_3N_4 or SiO_2) on a GaN film, then patterning the dielectric to produce openings of greater than a few microns wide that expose the underlying GaN film. When MOCVD is performed on the patterned sample under favorable conditions, adatoms only nucleate on the exposed GaN surface and not on the dielectric film surface. As the GaN film continues to grow above the window lateral overgrowth occurs with crystal facets that depend on process conditions (temperature, pressure, gas constituents) and the orientation of the opening with respect to the GaN crystal direction. Depending on the orientation of the dielectric mask opening, defects either bend towards the lateral facets [51] or reach the top GaN surface. Both scenarios are undesirable for the proposed GaN SJ technology, therefore a unique type of SAE called Aspect Ratio Trapping (ART) is utilized to trap defects inside the dielectric window opening. Filtering of dislocations has been reported in GaN nanostructures [25] for LED devices, but has not been applied to GaN devices with significant lateral epitaxy.

This chapter covers the process development of selective area epitaxy (SAE) for GaN on c-

plane Sapphire and Silicon (111) substrates. The goal is to reduce threading dislocations in the over-grown GaN films and fabricate electronic devices from the improved semiconductor material, while providing proper selectivity of the GaN growth. This means that GaN will only be deposited in the opening of the field dielectric and growth laterally from any film that grows above such a window, with no GaN deposition on top of the field dielectric. SAE process development started with HVPE GaN templates on Silicon (111) substrates purchased from Kyma Technologies. Important knowledge was gained about maintaining appropriate Nitrogen partial pressure during the initial temperature ramp such that the GaN template was not etching by the H_2 carrier gas. Then a SAE GaN-on-Sapphire process was developed based on the GaN films grown in the previous chapters by the LT-GaN experiments. Ohmic contacts and schottky diodes were fabricated from the SAE GaN-on-Sapphire films to extract contact resistance and the background doping concentration of the MOCVD process. Finally, a Aspect Ratio Trapping (ART) process was developed on Silicon (111) substrates that were obtained from Texas State University that already had 1.4 μm thick GaN with the appropriate nucleation, transition and buffer layers to ensure high quality epitaxial GaN. The ART process was developed to trap defects inside the selective epitaxy window the produce over-grown GaN films that are virtually free of threading dislocations. This was confirmed with TEM, then ohmic contacts and schottky diodes were fabricated from the ART-GaN films.

5.1 GaN-on-Sapphire

The GaN-on-Sapphire process began with approximately 200 nm of GaN growth by the process described in the previous chapter, cleaned with 1:1 HCl:DI for 5 minutes and was then coated with PECVD Si_3N_4 to act as the selective epitaxy mask. Contact lithography was performed with a Karl Suss MA-6 mask aligner and AZ5214E-IR photoresist (PR). The lithography process steps included a solvent rinse and dehydration bake at 120 °C for 2 minutes, followed by spinning on the PR at 4000 RPM for 40 seconds. A soft-bake at 120 °C for 2 minutes was performed followed by exposure using i-line light at a dose of 100 mJ-cm^{-2}. Development of the exposed photoresist was done in AZ726 developer for approximately 30 seconds followed by a 8 minute hard-bake at

135 °C. After hard-bake, the PECVD Si_3N_4 films were etched in BOE and the PR was removed with AZ400T PR stripper. Before SAE was performed on the samples, another 5 minute clean in 1:1 HCl:DI was performed before loading into the MOCVD.

5.1.1 SAE Process Development

The proposed GaN SJ and simulated structures have vertical sidewalls that simplify the calculation of total charge in a SJ column. Therefore, the goal of the SAE study on Sapphire was to achieve vertical sidewalls, a planar top surface and to maximize the lateral growth during SAE. This is measured by calculating the Lateral-to-Vertical Growth Rate (LTVGR) for the over-grown GaN films using cross-section SEM images. Furthermore, sharp corners should be avoided to avoid peak electric fields in these locations. Pressure and temperature of the MOCVD reactor are two factors that greatly influence the facets of the over-grown GaN films [52], with higher temperatures and lower pressures resulting in GaN films with smooth c-plane surfaces and vertical (11-20) surfaces. The results of varying the reactor pressure and temperature for the GaN-on-Sapphire SAE films are shown in Figure 5.1.

The LTVGR for the 950 °C samples at 15 Torr and 76 Torr were 0.67 and 0.45 respectively. The facets observed in the 15 Torr 950 °C sample are predominately (11-20) with a slight rounding at the edge before reaching the top (0001) plane. This is desirable for SJ that will be operated at high voltages because sharp corners result in area of high electric field, which lead to early device failure. When the pressure was increased to 76 Torr, vertical growth of the SAE structure increases which is attributed to a mass-transport limited growth regime common to MOCVD reactors. This increase in vertical growth reduces the LTVGR and increases the rounding of the edges between the (11-20) and (0001) surfaces. The LTVGR for the 820 °C samples at 15 Torr and 76 Torr were 1.3 and 0.75 respectively. The inclined plane (11-22) is now apparent at the lower temperature (820 °C) and there is no discernible (0001) surface in the overgrown region. The change in facets of the overgrown GaN are attributed to differences in surface energy, with the (11-22) surface being stable at low temperature and high pressure due to nitrogen polarity of the surface [52]. As the pressure of the reactor increased to 76 Torr at 820 °C, a hillock shaped top surface appears accompanied

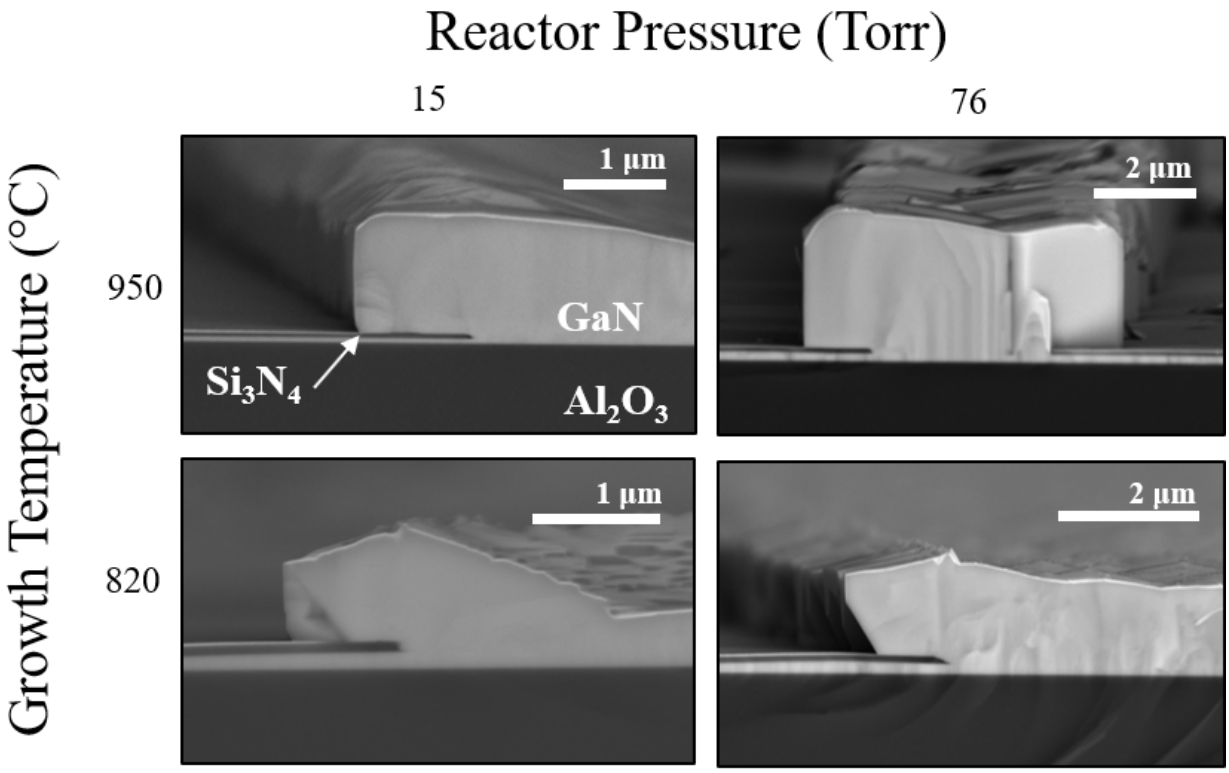

Figure 5.1: SEM images of GaN grown selectively using patterned Si_3N_4 on GaN-on-Sapphire. The reactor pressure and temperature were varied to study the over-grown region morphology. The samples were coated in a thin film of Au to facilitate SEM imaging.

by many sharp edges at the sidewalls of the overgrown region. The over-grown structures for the lower growth temperature are not desirable for the proposed SJ technology. Therefore, the reactor conditions of 15 Torr and 950 °C were chosen for future device processing and epitaxy development.

5.2 GaN-on-Silicon (111) Aspect Ratio Trapping

Current technology for GaN-on-Si (111) has a defect density of around 10^8 cm^{-2} - 10^{10} cm^{-2} depending on the buffer layers and processes used. The utilization of SAE has been proven to enhance device performance for Light Emitting Diodes (LEDs) and Laser Diodes (LDs), where specifically the LDs lifetime was increased by a significant amount due to the defect density reduction enabled by the SAE process. Threading dislocations will terminate at the top surface of a

GaN film and can act as trapping centers and create undesirable leakage currents. However, some really cool people were able to show that defects could be trapped in the windowed region of the SAE process by enabling a window that has an aspect ratio greater than one. This process has been applied to the Germanium and Silicon semiconductors and has been shown to work in the Nitrides as well. However, these reports only focus on LEDs and/or nano-wires that do not have significant lateral epitaxy, which is the goal of this research. This section covers the development of an ART process for GaN-on-Si (111) by utilizing E-beam Lithography (EBL) and an RIE process to transfer that pattern to the Si_3N_4 mask. The samples were first etching in RIE using SF_6 and Ar to remove the AlGaN layer that is approximately 20 nm thick and were subsequently coated with 150 nm of Si_3N_4.

5.2.1 E-beam Lithography and RIE Development

The EBL process development began with a dose test to ensure proper pattern transfer. Sample preparation for the dose test is shown in Figure 5.2(a). A Silicon (100) sample was prepare by degreasing in solvents and then depositing 150 nm of Si_3N_4 followed by spin coating of PMMA A4 at 3000 RPM for 40 seconds. A soft-bake at 185 °C was performed for 90 seconds. The sample was then loaded into a Tescan MIRA EBL system and pumped to base pressure of $5x10^{-6}$ Torr.

The accelerating voltage used was 30 kV and the different levels of dose were 250 μm/cm^2, 300 μm/cm^2, 350 μm/cm^2, 400 μm/cm^2 as shown in Figure 5.2(b). After exposure the sample was developed in an MIBK/IPA mixture for 60 seconds. Then the sample was loaded into a e-beam evaporator where 50 nm of Cr was evaporated. After deposition, the Cr layer on top of the PMMA A4 was lifted off using acetone, to leave behind the structures shown in Figure 5.2(b-c). The 250 μm/cm^2 dose structures were not continuous for the larger structures and none of the finer line widths were resolved. This is attributed to not providing sufficient dose throughout the thickness of the PMMA which results in a thin PMMA film left at the surface. This residual PMMA film lifts off all Cr that was deposited on top of it, which leaves behind no pattern after rinsing in acetone. When the dose was increased to 300 μm/cm^2 the thinner lines were resolved but the larger structures showed non-uniformity in the Cr thickness. A uniform dose and Cr thickness was observed for the

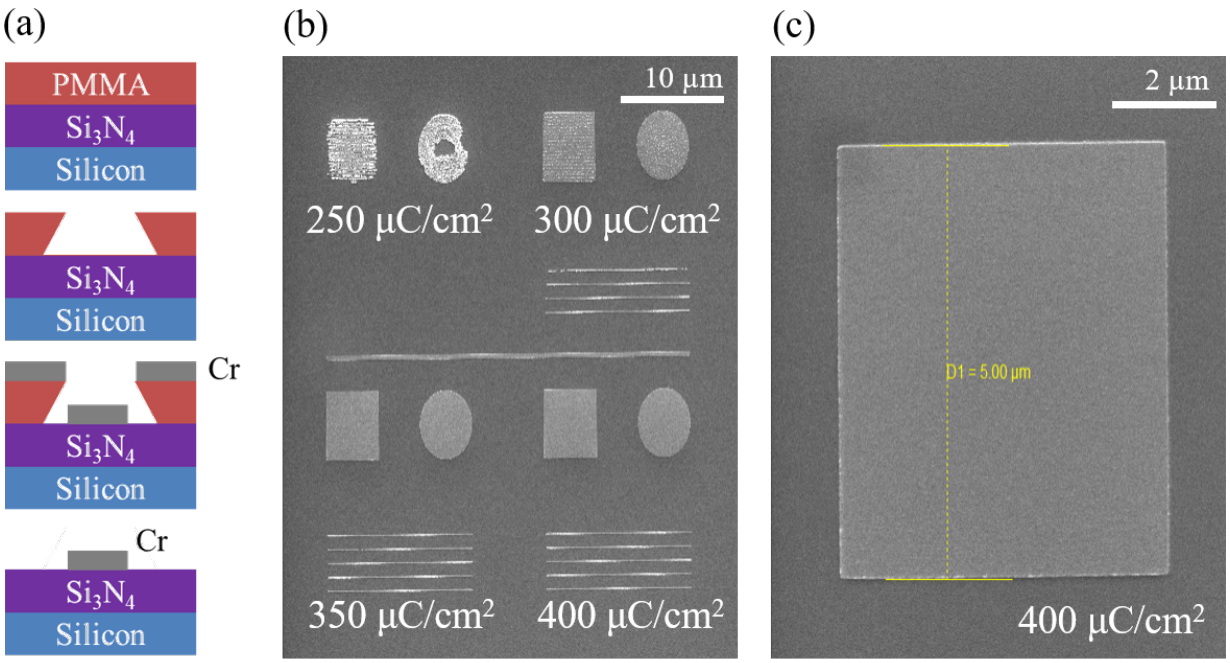

Figure 5.2: (a) Process flow used for the EBL process development (b) SEM of Cr films lifted-off on the Si_3N_4/Silicon (100) substrates for 4 different doses. (c) SEM of the 400 μC-cm^2 process showing proper pattern resolution and uniformity.

400 μm/cm^2 dose, which was determined appropriate for the desired process. After the dose test experiment was complete, the development of the ART process began. An aspect ratio of greater than 1 is required to successfully trap threading dislocations in the SAE window. The thickness of Si_3N_4 used in the ART process was 150 nm to ensure sufficient coverage and minimize the probability of pin holes that would allow for GaN deposition on the mask region. Therefore, lines with widths less than 150 nm must be realized after pattern transfer to meet the goal of achieving an aspect ratio greater than one. To study the impact of window opening on defect trapping, lines widths from 50 - 400 nm were drawn in the EBL and tested with the Cr lift-off process previously described. After lift-off the width of the lines was measured using the same Tescan EBL and the results are shown in Table 5.1.

After lift-off the measured window widths were close to those drawn by the EBL system for patterns greater than 100 nm, but were significantly larger for the 100 nm and 50 nm patterns.

Drawn (nm)	After Lift-off (nm)
50	80-90
100	130
200	210
400	405

Table 5.1: Comparison of the window width drawn using EBL and the measured width after the Cr lift-off process.

This is due to the classic lithography trade-off between the resist thickness and pattern resolution. Thinner PMMA A4 would enable higher fidelity between the drawn and measured structures, but in this process a thicker PMMA A4 film is desired to act as a hard mask during the RIE process. Therefore, since the thickness of the Si_3N_4 mask was chosen to be 150 nm, the results from this study were deemed acceptable. The 50 and 100 nm drawn lines would still enable a pattern in the PMMA that was less than the thickness of the Si_3N_4 mask such that an aspect ratio greater than 1 could be achieved. Pattern transfer from the PMMA to the underlying Si_3N_4 began with a BOE etch. However, due to the isotropic nature of the etch the aspect ratio requirement was not met. A thin Cr layer was then inserted between the PMMA and the Si_3N_4 to act as a hard mark for the subsequent dielectric etch. Again, due to the isotropic nature of both the Cr and dielectric etch, the aspect ratio requirement was not met. Therefore, an RIE process development began as shown in Figure 5.3(a). The process began with spin coating PMMA A4 on Sapphire substrates that had GaN grown as previously discussed in the other sections and a PECVD Si_3N_4 film. Lines of the width as outlined in Table 5.1 were drawn and the RIE process was performed with CHF_3 and O_2 at flows of 50 sccm and 5 sccm respectively. The pressure of the RIE was held at 20 mTorr, while the temperature was 18 °C and the RF and ICP powers were 50 W and 200 W respectively. The measured DC self-bias of the RIE process was recorded in the range of 290 - 320 V. The etch was performed for 6 minutes. The results of the RIE process for etch rate of Si_3N_4 and PMMA A4 are shown in Figure 5.3(b). The etch rate of the Si_3N_4 was calculated to be 0.65 Angstroms/sec and the etch rate of PMMA A4 was calculated to be 0.54 Angstroms/second resulting in a selectivity of 1.2. SEM cross-section images are shown in Figure 5.3(c) of the etched Si_3N_4 after the RIE

process. The samples were coated in Au to eliminate charging of the sample during SEM.

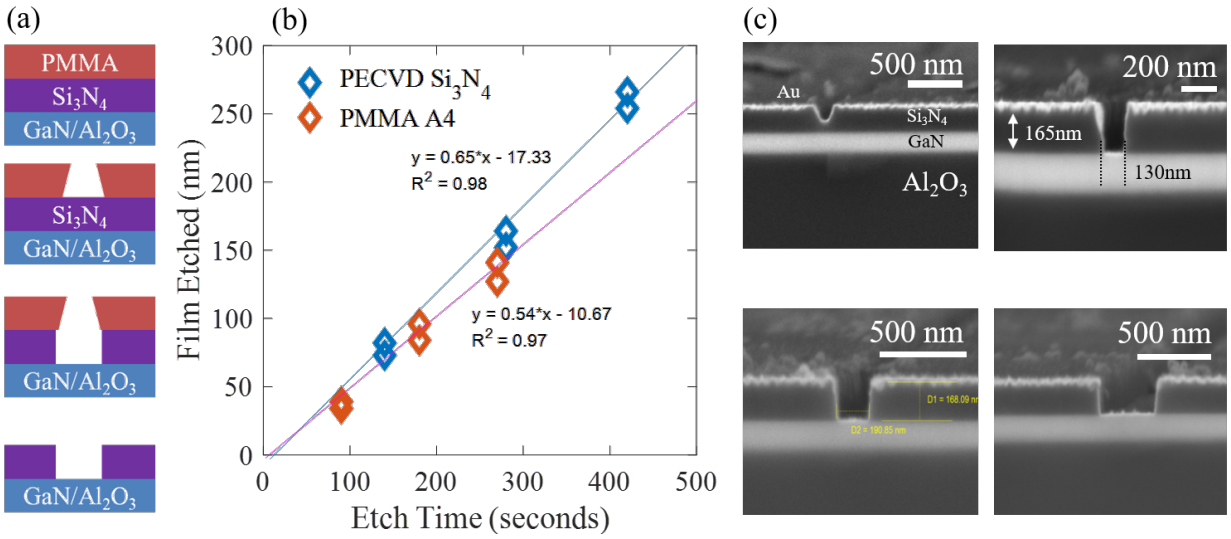

Figure 5.3: (a) Process flow used for the RIE dry etch recipe development for etching Si_3N_4 with a PMMA hard mask. (b) Etch rate of Si_3N_4 and PMMA measured used profilometry. (c) SEM cross-section of the windows etched in Si_3N_4 on GaN/Sapphire films using the RIE recipe previously developed.

From the images shown in Figure 5.3(c), it can be seen that the 50 nm draw windows did not completely transfer the pattern throughout the entire Si_3N_4 film. One possibility is that the smaller window size sees limited etching species, thus taking longer to etch than larger structures. Another possibility is that a thin PMMA layer was left after development which acted as a mask for the beginning of the etch process. The 100, 200 and 400 nm draw windows were able to etch completely. The 100 nm window was able to meet the goal of achieving and aspect ratio greater than one, and was measured at 1.26. This is acceptable to be used for the ART process and will be used in the following section. A longer etch time of 7 minutes was used in all subsequent processes to ensure that the 50 nm window had proper pattern transfer.

5.2.2 ART Process Development

The development of a SAE process for growing GaN on Sapphire substrates has been presented. The proposed GaN SJ technology should be developed on Silicon substrates to help reduce manufacturing costs. The process conditions from the GaN-on-Sapphire SAE structures (920 °C and 15 Torr) serve as a starting point for the development of an ART process from the nano-structure opening in the Si_3N_4 window. The morphology of GaN using SAE is dependent upon the window size [53], the window orientation [54], the flow rate of TMGa [55] and other factors. The most important of which is the window orientation when a rectangular cross-section of the GaN over-grown structure is desired. Figure 5.4 shows top-down SEM images of (a) lines along the <11-20> direction (b) dots of varying diameter and three ring structures and (c) an inclined image of lines along the <11-20> direction.

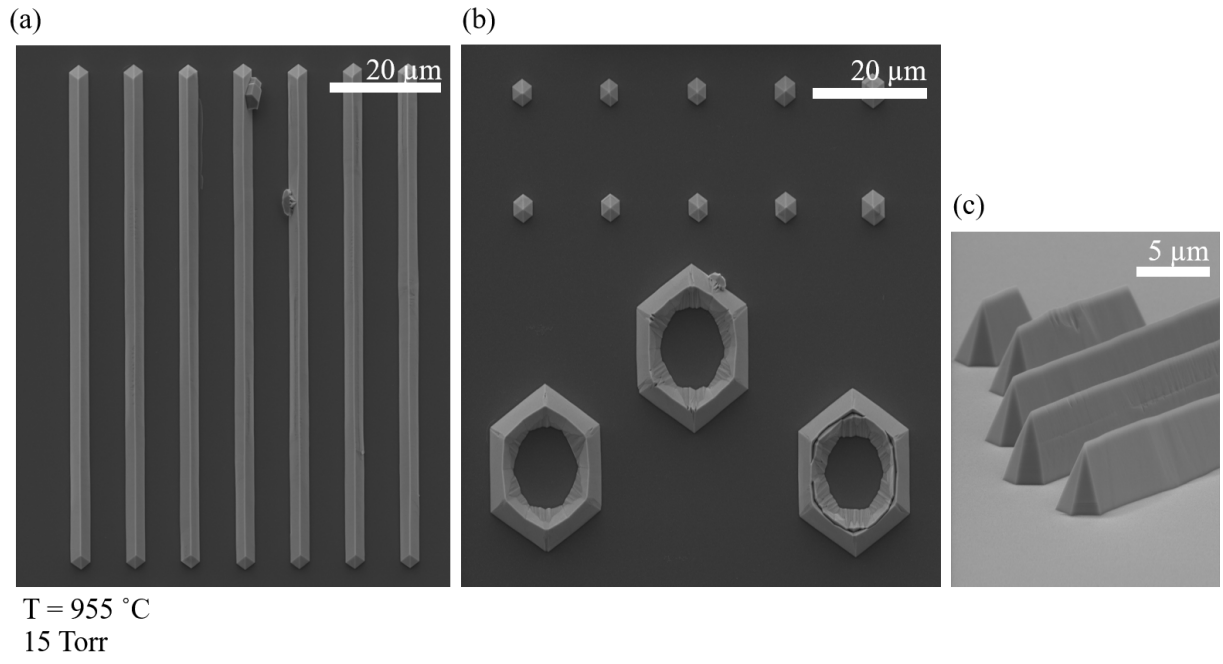

Figure 5.4: Top-down SEM of SAE GaN films using the EBL process. (a) top down image of GaN structures grown with lines oriented in the <11-20> direction (b) top-down image of GaN grown from dots and ring structures of varying inner diameter (c) inclined image of GaN structures with window openings aligned along the <11-20> direction.

The MOCVD process was performed at 15 Torr and 955 °C for 15 minutes. Smooth (11-22) surfaces are apparent in the GaN structures shown in Figure 5.4(a). Growth defects are observed on the fourth and fifth GaN structures when counting from the left. However, the lack of GaN deposition of the Si_3N_4 mask suggests that the selectivity of the process appears to be sufficient. Further support of this claim is apparent in Figure 5.4(b) where no GaN deposition on the mask is observed. Two rows of dots with diameters from 50 nm to 200 nm were patterned with the EBL process. The GaN morphology is hexagonal is nature with a pyramidal cross-section. Three different ring structures were patterned with EBL with a fixed outer diameter and varying the inner diameter. For the left most and center ring structure, uniform hexagonal GaN morphology is observed. However for the right most ring structure, the inner diameter has been reduced such that a seam appears at the top most portion of the GaN structure. This is attributed to limited mass transport to the inner area, resulting in a slower growth rate. Different lengths of the stripes along the <11-20> direction are shown in Figure 5.4(c). No discernible difference in GaN morphology is apparent when the length of the window is changed, nor any dependence due to proximity of the stripes. A cross-section image of GaN structures grown from lines oriented in the <1-100> direction are shown in Figure 5.5(a).

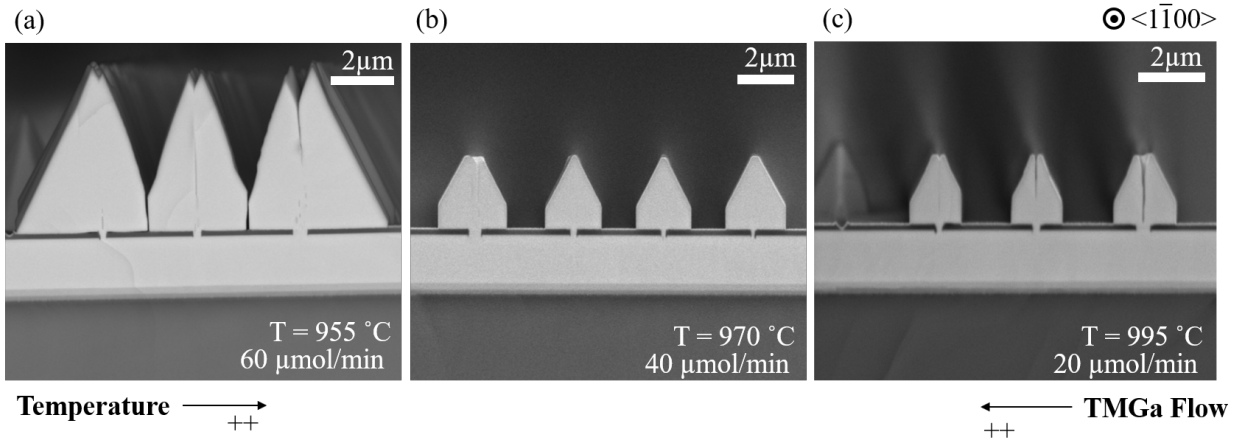

Figure 5.5: Cross-section SEM of GaN grown along the <1-100> direction from 50, 100, 200 and 400 nm wide openings in Si_3N_4 at different temperatures and TMGa flow rates.

A triangular cross-section is apparent for the GaN structures with a seam appearing at the center of the window. Furthermore, a strong dependence on the sidewall morphology is observed for structures that share a side with another growing GaN film. The GaN structures form a quasi-vertical facet where to films meet and do not fully coalesce. This is attributed to limited adatoms being able to reach these surfaces and the predominant (11-22) surfaces being a sink for most of the available adatoms. The underlying GaN and AlGaN buffers layers are apparent in all three cross sectional images shown in Figure 5.5. The bottom most layer is the Silicon (111) substrate, followed by a thin AlN layer, two thin $Al_xGa_{1-x}N$ layers and the thick GaN buffer layer. The growth rate for the GaN structures in Figure 5.5(a) is greater than 10 μm/hr, which would make precise deposition of a 500 nm layers for the SJ structure difficult. Therefore, the growth rate is reduced by lowering the TMGa molar flow rate from 60 μmol/min to 40 μmol/min. Also, there was no discernible (11-20) vertical facet for the outermost GaN films, so the reactor temperature was increased to promote growth of the vertical facets. The growth rate was reduced to approximately 8 μm/hr and the appearance of the vertical (11-20) facet and a small top (0001) surface is apparent for the process shown in Figure 5.5(b). However, for the proposed GaN SJ technology it is desired to have no inclined (11-22) facets, so the reactor temperature was further increased and the flow rate was reduced to 20 μmol/min as shown in Figure 5.5(c). A wider (0001) surface was observed but a seam appeared at the center of every window. This is not desirable for the proposed technology so the process conditions as shown in Figure 5.5(b) were used in future experiments. A rectangular film cross-section is desired for the proposed GaN SJ, but increases in temperature and reduction is the TMGa flow rate result in undesirable GaN morphology. Therefore, NH_3 flow modulation was investigated due to being shown to have an impact on SAE GaN morphology [56] and provide films with LTVGR of greater than 4. The results of the pulsing NH_3 experiment are shown in Figure 5.6.

The TMGa molar flow was varied between two values, 20 μmol/min and 40 μmol/min, while the ON-OFF times for the NH_3 flow were 30 seconds - 5 seconds (30/5) and 20 seconds - 15 seconds (20/15). The frequency of cycling was kept constant while the duty cycle was changed.

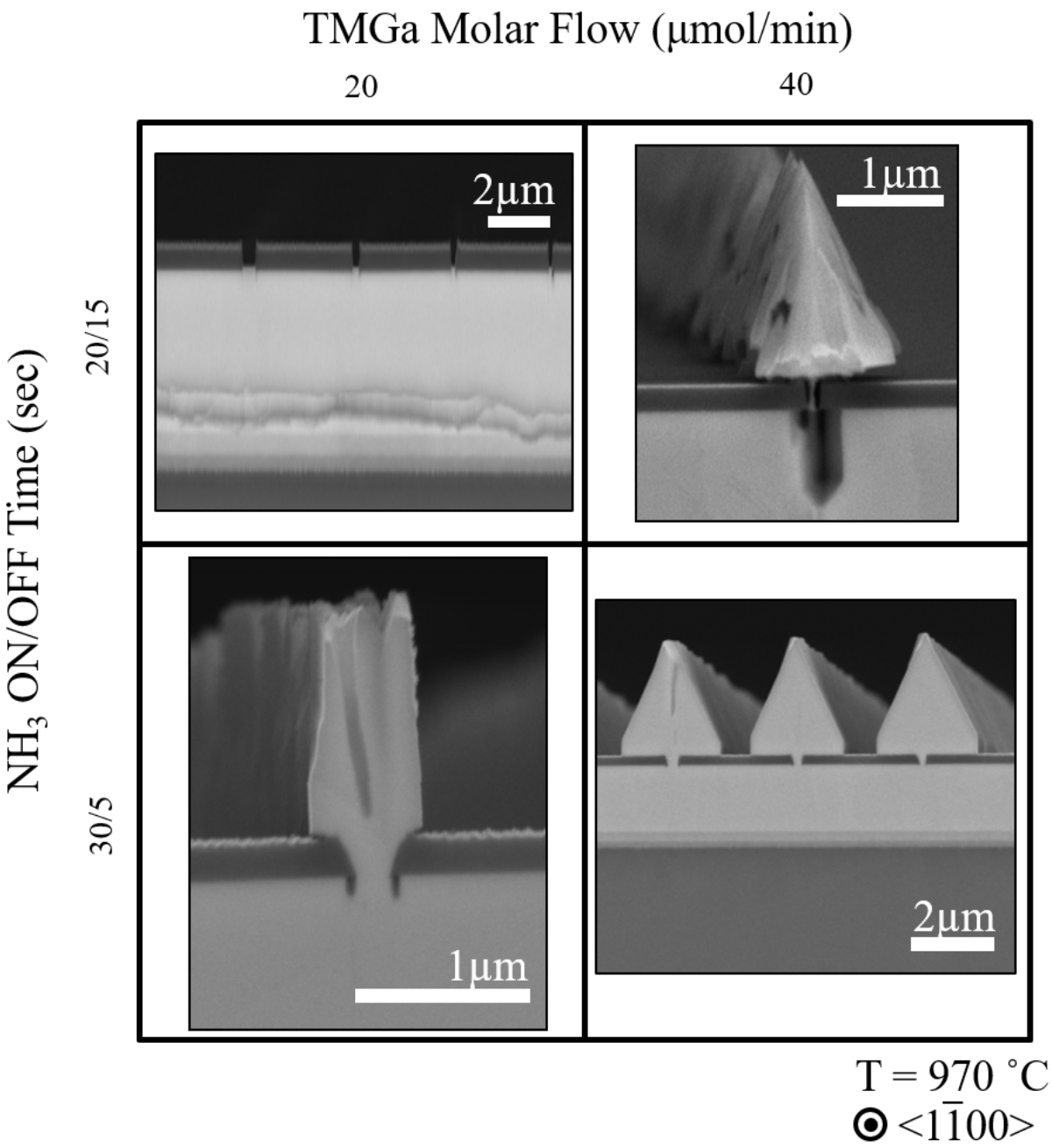

Figure 5.6: Cross-section SEM of GaN grown using pulsed NH_3 flow during growth.

The lowest condition did not have any GaN grown from the windowed regions of Si_3N_4. This is because while the NH_3 was off for 15 seconds, the H_2 environment was able to etch any GaN that had been grown during the on-cycle of 20 seconds. Therefore, the molar flow rate of the TMGa

was increased to 40 μmol/min and GaN deposition was observed. However, significant etching still occurred during the growth due to the long off-cycle time. The ON/FF time was then changed to 30/5 so that GaN etching would not occur. However, what appears to be dislocations stopping growth still show up for the lowest TMGa molar flow at the 30/5 ON/OFF time. While the sidewalls of the growth appear vertical, the rest of the SAE structure is compromised such that a useful device could not be made. When the molar flow rate was increased to 40 μmol/min, a similar cross-section is observed for the structures that were not exposed to the NH_3 pulsing experiment. Therefore, the pulsing experiments were abandoned and the structures in Figure 5.5(b) were utilized for future device and process development. Now that a process has been chosen, it is important to verify that the defects are being trapped at the interface. TEM sample preparation was performed using a Tescan FIB/SEM with assistance from Jon Anderson at Texas State University.

5.2.3 TEM of ART GaN

Cross-sectional TEM has been used extensively to investigate defect structures in GaN films grown using SAE [57]. Pure-edge dislocations, screw dislocations and mixed dislocations have been found in GaN films with Burgers vectors 1/3<11-20> [58] [59], <0001> and 1/3<11-23> respectively. The invisibility criterion states that if the dot product of the reflection vector used for imaging, g, and the Burgers vector of a dislocation is zero then the dislocation is out of contrast. Bright field and dark field images of the ART GaN structures were taken along with two zone axes, g = 0002 and g = 11-20. The TEM images of ART GaN that was grown from the 50 nm draw lines in EBL are shown in Figure 5.7.

The bright field image in Figure 5.7(a) shows how threading dislocations in the underlying GaN layer are terminated at the GaN surface that is covered in Si_3N_4 and that no threading dislocations are observed in the ART-GaN. This highlights the benefit of growing GaN selectively from nano-scale windows due the lower probability that a threading dislocation will propagate into the overgrown region. Moire fringes are observed for the two dark field images shown in Figure 5.7(b-c). The dark field image in Figure 5.7(b) with g = <0002> has mixed and screw dislocations in contrast. There appear to be no mixed or screw dislocations in the ART GaN structure.

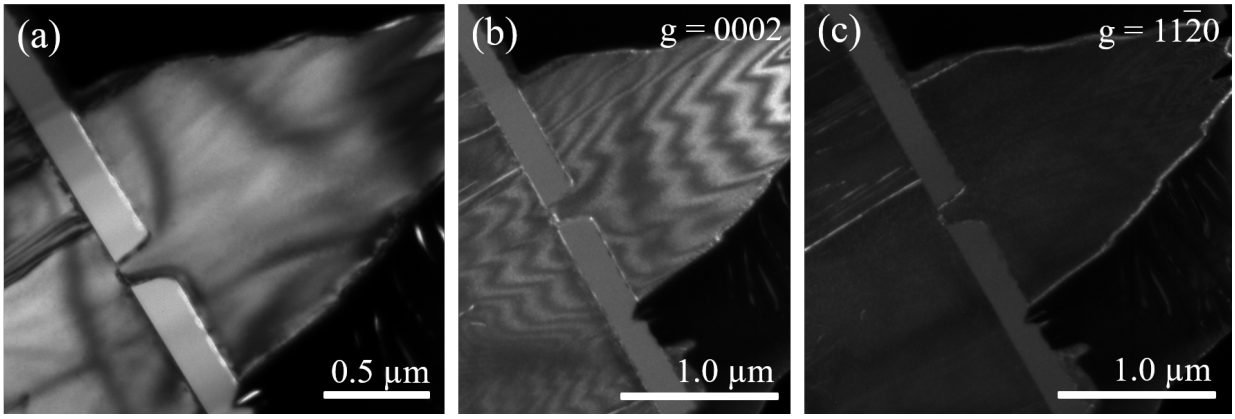

Figure 5.7: (a) Bright field TEM of windows for selective epitaxy. (b) Dark field TEM with zone axis = 0002 to highlight mixed and screw dislocations (c) Dark field TEM with zone axis = 1120 to highlight mixed and edge dislocations

Figure 5.7(c) shows a dark field TEM image with g = <11-20> that highlights mixed and edge dislocations. Again, no mixed or edge dislocations are observed in the ART GaN structure. The TEM images for ART-GaN grown from 100 nm windows drawn in the EBL are shown in Figure 5.8. The bright field image shows dislocations inside the window that start from the GaN surface bend and terminate at the sidewalls of the windowed region.

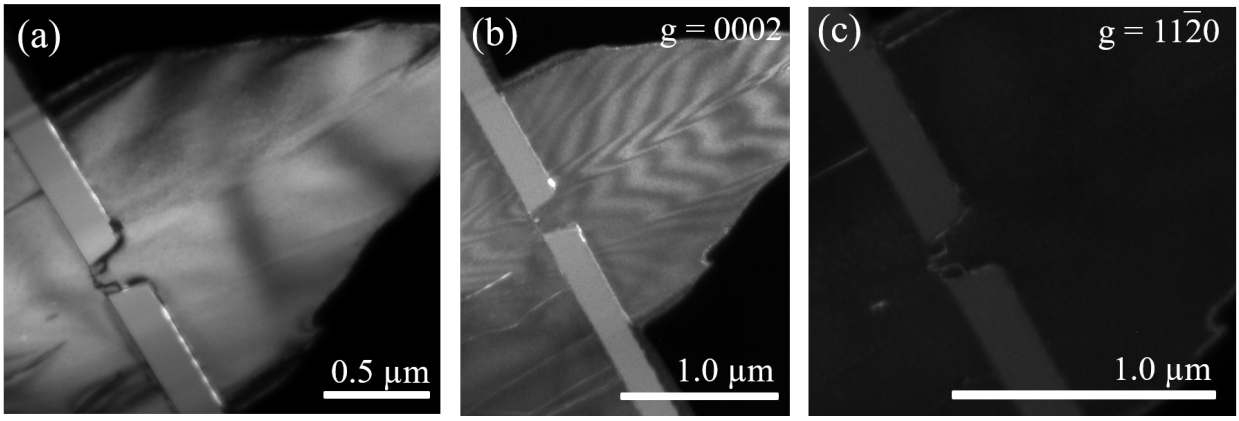

Figure 5.8: (a) Bright field TEM of windows for selective epitaxy. (b) Dark field TEM with g = <0002> to highlight mixed and screw dislocations (c) Dark field TEM with g = <11-20> to highlight mixed and edge dislocations

The threading dislocations that appear in the bright field image are do not appear in the dark field image with zone axis one, but they do appear in the dark field image of zone axis two. This means that the threading dislocations are pure edge dislocations. This is exciting because this is proof that the ART process on GaN works and that no threading dislocations propagate into the over-grown GaN. The TEM images for ART-GaN grown from 200 nm windows drawn in EBL are shown in Figure 5.9. This structures do not have an aspect ratio greater than one and the threading dislocations are able to make their way into the over-grown GaN regions. However, it is interesting that some annihilation still occurs inside the windowed region.

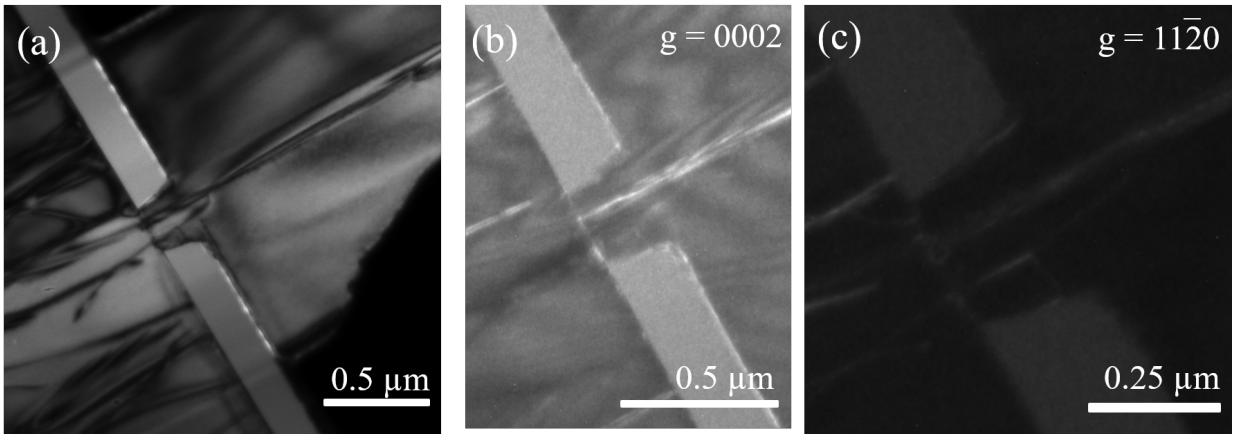

Figure 5.9: (a) Bright field TEM of windows for selective epitaxy. (b) Dark field TEM with g = <0002> to highlight mixed and screw dislocations (c) Dark field TEM with g = <11-20> to highlight mixed and edge dislocations

Since some of the threading dislocations appear in both the dark field images, this means that these dislocations are mixed type (edge + screw). This study successfully employed ART-GaN and showed that lines drawn in the <1100> crystal direction can trap threading dislocations when a proper aspect ratio of the dielectric window is utilized.

6. P-TYPE GALLIUM NITRIDE

The first reports of p-type GaN (p-GaN) [60] [61] and resulting p-n junction Light Emitting Diodes (LEDs) describe using Magnesium (Mg) as the dopant in an MOCVD process. The key to realizing p-type conduction was the utilization of a low-energy electron-beam irradiation (LEEBI) process that produced hole concentrations of approximately 10^{16} cm^{-3} at room temperature. However, other researchers were unable to re-produce the low resistivity p-GaN films with the LEEBI process. Later, it was discovered that low-resistivity p-GaN could also be achieved by a thermal anneal in nitrogen ambient at temperatures above 700 °C [62]. The thermal anneal activates the Mg dopants that were passivated with hydrogen during MOCVD growth [63] [64] [65]. The activation energy (E_A) for Mg acceptors in GaN ranges between 160 - 200 meV [66] [67] [68] with a decrease in E_A observed for films with higher doping levels [69]. This phenomenon is well reported for other semiconductors and could have many causes [70] [69]. Despite being a relatively shallow acceptor, the E_A of Mg in GaN relative to kT at 300K (26 meV) results in p-GaN films that have low activation efficiencies (typically 1%) and subsequently low conductivities. Furthermore, self-compensation mechanisms of Mg in GaN with nitrogen vacancies limit the hole density to approximately 10^{18} cm^{-3} [71]. However, as described in the Simulation section, the proposed GaN SJ technology requires doping densities in the range of 10^{16} - 10^{17} cm^{-3} for the SJ channels. To minimize the metal contact resistance between, highly doped p-GaN and n-GaN structures are included at the ends of the SJ structure. Despite the previously discussed issues with obtaining low-resistivity p-GaN, reasonably low specific contact resisitivites (<10^{-4} Ω-cm^{-2}) to p-GaN have been reported [72] [73] [74] [75] with doping densities of 10^{17} - 10^{18} cm^{-3}.

The section begins with a baseline ohmic contact that involves a Ni/Au metal scheme to commercial p-GaN purchased from a vendor. Once an ohmic process is established, a Mg inter-layer between the p-GaN and the Ni is studied to see if Mg will increase the surface doping concentrations enabling a reduction in contact resistance. Diffusion studies have shown that annealing evaporated Mg on n-type GaN results in p-GaN after anneal [76] [77]. Furthermore, an increase

in doping of p-GaN by Mg diffusion has been demonstrated [78]. Talk about what studies have already been done with Mg, ohmic study with Ni-Mg evaporated with 8 percent Mg by weight with Pt contact on top , diffusion studies and XPS/UPS results. Diffusion of Mg to make p-GaN [76] and [77] with XPS [78] showing fermi level changing.

6.1 Baseline Ohmic Contact Process

Enabling a low resistance ohmic contact to p-GaN is an important goal to realize GaN superjunctions. Simulations presented herein have shown that the p-GaN contact resistance is one of the most important parameters to minimize R_{ON} of a superjunction diode. Typical contact resistivity values range from 10^{-4} Ω-cm^2 - 10^{-6} Ω-cm^2 depending on the metals used. To date, the Ni/Au metal scheme has produced the lowest contact resistivity value of 4.6x10^{-6} after an oxygen anneal. The mechanism for creating a low resistance ohmic contact to p-GaN involves the oxidation of the Ni and diffusion of the Au to the p-GaN interface [79] [80] [81]. The following baseline Ni/Au ohmic contact process was developed to p-GaN on a Al_2O_3 substrate purchased from a vendor. The specifications given for the p-GaN are as follows: The resistivity was < 0.5 Ω-cm with dislocation densities below 10^8 cm^{-2} and a Mg concentration of 1x10^{19} cm^{-3}. Hall measurements of the p-GaN produced a hole concentration of 1.5x10^{17} with a hole mobility in the range of 5 - 10 cm^2/Vs. The measured resistivity from the Hall measurements was 5 Ω-cm, which is greater than an order of magnitude higher than the vendor specification. WDS measurements indicate that the Mg concentration of the vendor p-GaN was 3.47x10^{19} +/- 0.38 cm^{-3}.

Baseline process development for the Ni/Au ohmic contact to p-GaN began with a surface pre-clean of BOE. Then, a lift-off lithography process was performed which entailed spinning on LOR-3A at 2000 RPM for 40 seconds, followed by an 8 minute soft-bake at 165 °C. Next, AZ5214 photoresist was spun on at 4000 RPM for 40 seconds and then soft-baked at 120 °C for 2 minutes. Contact lithography was performed using a dark field mask of the TLM structures and the sample was exposed to a dose of 100 mJ-cm^{-2} of i-line light. After exposure, development of the AZ5214 and LOR-3A was performed using AZ726 for 2 minutes 30 seconds. A hard bake at 135 °C for 8 minutes was then performed to harden the photoresist such that it would withstand

a subsequent acid surface pre-clean. Samples with no pre-metallization clean, 1:1 HCl:DI, and BOE were fabricated with only the BOE sample resulting in ohmic contacts. Next, the samples were loaded into a Lesker e-beam evaporator to deposit the 25 nm of Ni. After Ni deposition, the samples were then transferred to a DC sputter system to deposit 25 nm of Au. Lift-off was performed with AZ400T and the TLM structures were measured using the HP4155B parametric analyzer. As deposited high resistance was observed so then the samples were annealed at 350 °C, 400 °C, 450 °C 500 °C for 5 minutes each at 30 Torr with a constant flow of air. The results of the 500 °C TLM data are shown in Figure 6.1. The as deposited contacts were schottky in nature and had a voltage offset of approximately -0.25V due to the schottky barrier formed between the Ni and p-GaN interface.

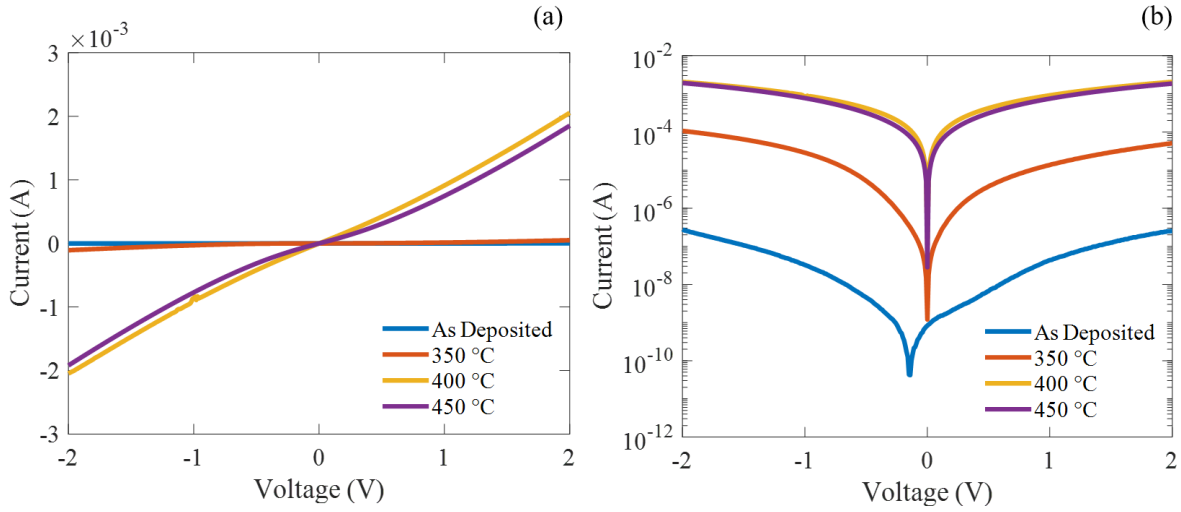

Figure 6.1: (a) Linear I-V plots of Ni/Au ohmic contacts to pGaN after different anneal temperatures (b) Log(I)-V plots of the same data shown in (a)

After the 350 °C anneal, the current increases by approximately 100x and the not does exhibit a schottky barrier offset. However, not until anneal above 400 °C is a linear I-V relationship observed, accompanied by another order of magnitude increase in current relative to the 350 °C anneal condition. Upon further anneal of the sample beyond 400 °C the relationship between I-V

becomes sub-linear for some of the contacts. Microscope images before and after anneal as well as a TLM plot of the 500 °C anneal sample is shown in Figure 6.2. The change in color of the metal stack from orange to purple is attributed to the oxidation of the Ni to form NiO as well as the diffusion of the Au to the interface of the p-GaN. The TLM plot for the 500 °C anneal shows an R^2 factor of 0.86, which is significantly less than typical values for TLM plots which are usually greater than 0.95. This means that 14% of the variance associated with the data cannot be explained due to the TLM method. The 350 and 400 °C anneal samples did not provide R_2 values greater than 0.5 so that have not been included. The low R_2 values observed can be attributed to the non-linearity of the I-V measurements for the Ni/Au contacts. The R^2 value for individual I-V current measurements ranged from 0.970 to 0.990 for these devices, whereas ohmic contacts that produce more linear TLM plots typically have R^2 values of at least 0.999 for an individual I-V measurement.

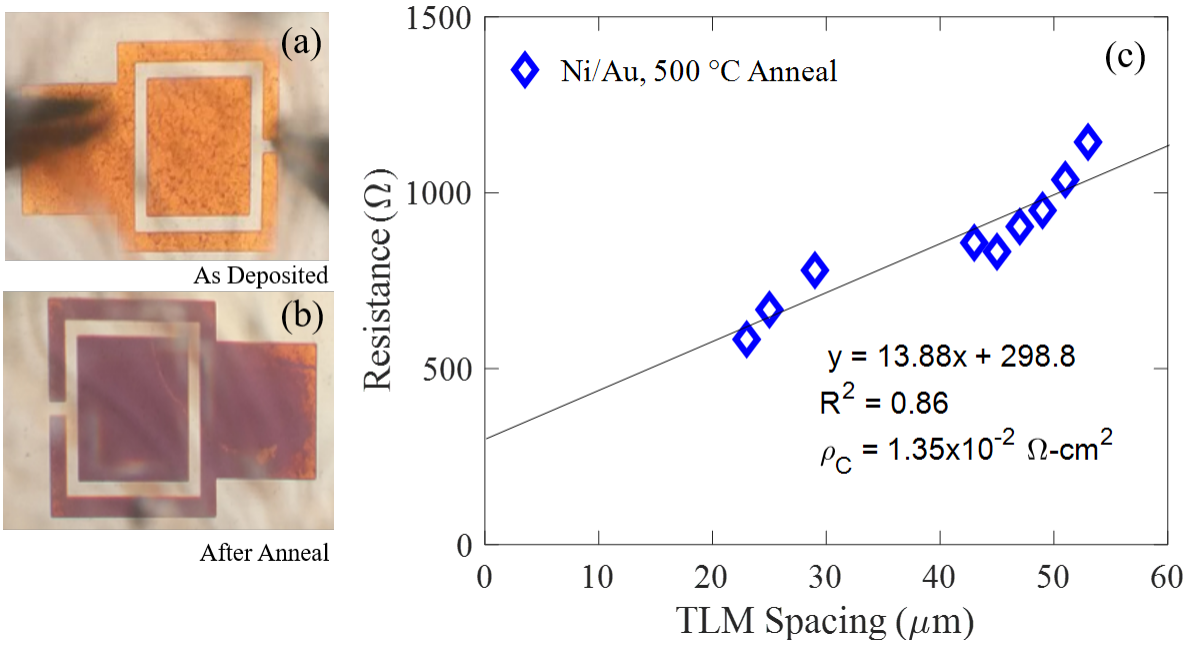

Figure 6.2: (a-b) Microscope images of Ni/Au ohmic contacts to p-type GaN (a) before and (b) after anneal in air. (c) TLM plot for the Ni/Au contacts to p-type GaN after 500 °C anneal

Table 6.1 summarizes the baseline ohmic contact development and resulting characteristics for the Ni/Au metal stack. The sheet resistance of the sample appears to decrease as the anneal temperature is increased, however using the statistical program R and a Tukey comparison is made that verifies there is no significant different in the slopes. Similarly, any changes in the transfer length of specific contact resistivity are within the error of the linear regression.

T_A °C	R_{SH} (kΩ-sq)	L_T (μm)	ρ_C (Ω-cm^2)	R^2
450	12.5 ± 4.2	10.76 ± 2.0	1.447x10^{-2} ± 1.06	0.79
500	11.3 ± 4.1	10.76 ± 2.7	1.351x10^{-2} ± 1.16	0.86
550	10.8 ± 7.5	14.11 ± 11.0	2.156x10^{-2} ± 2.12	0.67

Table 6.1: Comparison of the baseline Ni/Au ohmic contact properties after anneal with ± values corresponding to a 95% confidence interval.

Different surface pre-treatments could potentially improve the ohmic contact properties for the Ni/Au stack. Furthermore, all previously published Ni/Au ohmic contacts deposit the Ni and Au without breaking vacuum while the baseline Ni/Au process developed here required an evaporation of Ni and a DC sputter of Au. To minimize the on-state resistance of a superjunction diode, improvements to the specific contact resistivity are required. The next section discusses and experiments with including a thin Mg layer between the p-GaN and Ni with the intent of improving the specific contact resistivity.

6.2 Mg inter-layer Study

A comprehensive review ohmic contact theory is not presented here, but can be found elsewhere [47]. The work function of a metal, ϕ_M, that is in contact with a semiconductor should define a barrier height, ϕ_B, that follows the relationship:

$$\phi_B = \phi_M - \chi \tag{6.1}$$

where χ is the electron affinity of the semiconductor. However, the calculated barrier heights

for different metals on common semiconductors, such as Silicon, Germanium, Gallium Arsenide and III-Nitrides, is relatively independent of ϕ_M [82]. While the underlying mechanism is not fully understood to date, the quality of the semiconductor surface is important when developing an ohmic contact. Therefore, it is difficult to control the barrier height between the metal and semiconductor. The barrier width between the metal and semiconductor depends on the doping concentration at the semiconductor surface. Current conduction mechanisms between the metal and semiconductor are thermionic emission, and tunneling or a combination of both. Semiconductors with sufficiently high doping will allow for carriers to tunnel directly from the metal to the semiconductor. Therefore, increasing the doping of the semiconductor surface directly under the contact would improve the specific contact resistivity. Mg is the dopant used to create p-GaN and has been included in ohmic metal stacks to p-GaN previously. However, these studies only produce contact resistivities values on the order of 10^{-5} Ω-cm^2, with the simpler Ni/Au stack producing lower contact resistivities by an order of magnitude. Specifically, these people used a Ni evaporation source that contained 8 $\%$ Mg by weight followed by a thin Pt layer [83].

The Mg inter-layer study used the same procedure for making the baseline Ni/Au. A surface pre-clean in BOE was performed, followed by lift-off lithography with LOR-3A and AZ5214. Before metallization the samples were exposed to a 5 minute clean in BOE. Different thicknesses of Mg were deposited (3nm, 8nm, 12nm, 20nm) with each being capped by 25 nm of Ni. Then 25 nm of Au was deposited on the samples by DC sputter and the lift-off was completed by putting the samples in AZ400T at 90 °C for 5-10 minutes. The TLM plots for the Mg inter-layer study are shown in Figure 6.3.

The 3 nm Mg sample does not show any change in sheet resistance, transfer length or specific contact resistivity with temperature. However, the 8nm Mg sample does show a significant sheet resistance change when comparing the slopes after 350 °C anneal to the sheet resistance for the 450 °C and 500 °C anneal. The 12 nm Mg sample did not have TLM data with an R^2 value greater than 0.5 for anneals under 450 °C so that data is not shown here. The 20nm Mg sample also did not show any significant change in sheet resistance, transfer length or specific contact resistivity

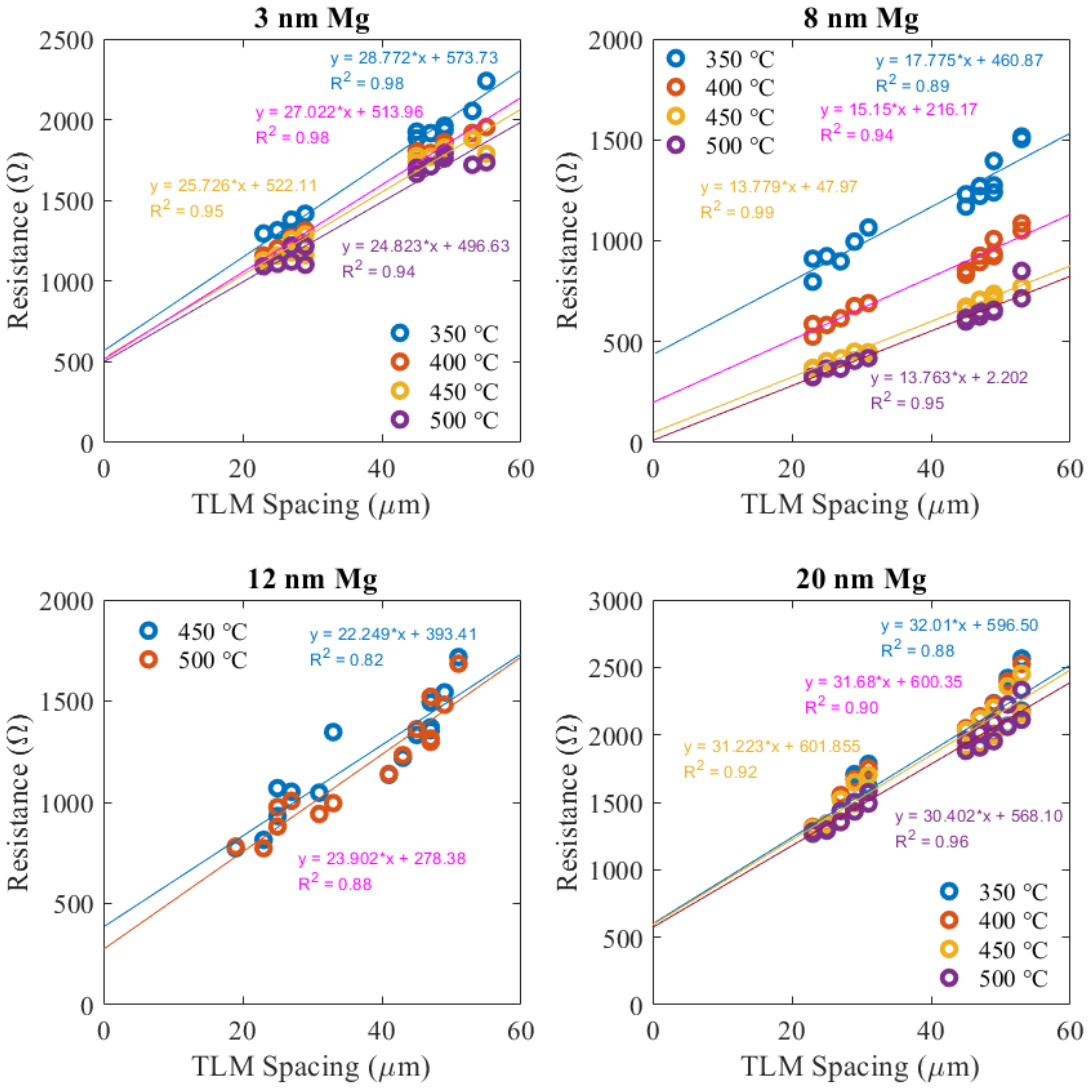

Figure 6.3: TLM study for different Mg thicknesses between the pGaN and the Ni/Au (25 nm/25 nm) metal stack (a) 3 nm Mg TLM plot (b) 8 nm Mg TLM plot (c) 12 nm Mg TLM plot (d) 20 nm Mg TLM plot

between any of the anneals. Comparisons of TLM plots is done with the statistical programming language R using multiple linear regression models. The linear regression model assumptions of linearity, normality of residuals and homogeneity of variances were tested with ANOVA, the Shapiro-Wilk (SW) normality test and the Brown-Forsyth (BF) test respectively for each TLM regression. For all TLM linear regressions, the R^2 values can be found on Figure 6.3. All linear

regressions had an R^2 value greater than 0.82, therefore the linearity assumption on all TLM linear regressions was considered to be valid. Furthermore, power calculations were made for each of the Mg thicknesses. The power for the multiple linear regression models were all greater than 0.80. For the 3nm Mg sample, the SW p-value was 0.97, 0.34, 0.12 and 0.11 for the 350 °C, 400 °C, 450 °C and 500 °C anneal respectively. Therefore, normality of the residuals assumption was considered to be valid at a significance level of α = 0.05 for rejecting the null hypothesis. For the 3nm Mg sample, the BF p-value was 0.99, therefore the assumption of variance homogeneity was considered to be valid at a significance level of α = 0.05. A multiple regression linear model was applied to the data for the 3nm and multiple comparisons were made to determine if the anneal temperature had a statistically significant impact on the slope and intercept of each TLM linear regression. Because multiple hypotheses are being tested, the Family-Wise Error Rate (FWER) must be taken into account and a Tukey pairwise comparison was made for the slopes. None of the comparisons between the temperature anneals had a p-value less than α = 0.05, therefore no significant difference in slopes are observed for the 3nm Mg sample. To compare the intercepts, a Bonferroni procedure was used for making 6 comparisons of all the intercepts for the different anneal temperatures. Therefore the p-value to determine statistical significance is adjusted to p = 0.05/6 = 0.00833. Difference contrasts were made to test the null hypothesis of H_0: β_1 - β_2 = 0, where β_1 and β_2 are the intercept estimates from the linear regression for two different anneal temperatures. All contrasts had p-values above 0.078, the null hypothesis was accepted that there is no statistical significant between the intercepts of the linear regressions for the 3nm Mg sample. Computation of the sheet resistance of each TLM plot entails multiplying the slope estimate from the linear regression by 840, which represents the total width of the metal contact in microns. The confidence interval on the sheet resistance is calculated directly from the confidence interval of the slope estimation of the linear regression model. The transfer length is calculated by taking the absolute value of the quotient between the intercept and slope. This value is then divided by 20,000, which represents the conversion from microns to centimeters and includes a factor of 2 to take care of the 2*L_T term from the x-intercept. The confidence interval on the transfer length

is calculated. The specific contact resistivity, ρ_C, is the product of the sheet resistance and the square of the transfer length as previously discussed. The confidence interval on ρ_C is calculated. A summary of all the TLM parameter extractions are shown in Table 6.2.

3 nm Mg TLM Parameters				
T_A °C	R_{SH} (kΩ-sq)	L_T (μm)	ρ_C (Ω-cm^2)	R^2
350	24.16 ± 2.16	9.97 ± 1.0	2.40x10^{-2} ± 0.65	0.98
400	22.69 ± 1.75	9.51 ± 0.9	2.05x10^{-2} ± 0.51	0.98
450	21.61 ± 3.07	10.1 ± 1.6	2.23x10^{-2} ± 0.89	0.95
500	20.851 ± 3.39	10.0 ± 1.9	2.09x10^{-2} ± 0.96	0.94
8 nm Mg TLM Parameters				
T_A °C	R_{SH} (kΩ-sq)	L_T (μm)	ρ_C (Ω-cm^2)	R^2
350	14.93 ± 2.89	13.0 ± 1.2	2.51x10^{-2} ± 1.0	0.89
400	12.72 ± 1.67	7.13 ± 1.5	6.48x10^{-3} ± 3.5	0.94
450	11.57 ± 0.47	1.74 ± 0.73	3.51x10^{-4} ± 2.5	0.99
500	10.72 ± 0.44	1.26 ± 0.8	1.70x10^{-4} ± 1.4	0.99
12 nm Mg TLM Parameters				
T_A °C	R_{SH} (kΩ-sq)	L_T (μm)	ρ_C (Ω-cm^2)	R^2
450	18.68 ± 5.0	8.8 ± 2.2	1.46x10^{-2} ± 1.1	0.82
500	20.07 ± 4.2	5.8 ± 2.3	6.81x10^{-3} ± 6.0	0.88
20 nm Mg TLM Parameters				
T_A °C	R_{SH} (kΩ-sq)	L_T (μm)	ρ_C (Ω-cm^2)	R^2
350	26.88 ± 4.7	9.3 ± 1.6	2.33x10^{-2} ± 1.2	0.88
400	26.61 ± 4.3	9.4 ± 1.4	2.39x10^{-2} ± 1.1	0.90
450	26.22 ± 3.7	9.6 ± 1.3	2.44x10^{-2} ± 1.0	0.92
500	25.53 ± 2.3	9.3 ± 0.87	2.23x10^{-2} ± 0.6	0.96

Table 6.2: Comparison of the baseline Ni/Au ohmic contact properties after anneal with ± values corresponding to a 95% confidence interval.

The 8nm Mg sample SW p-values were 0.26, 0.64, 0.24 and 0.14 for the 350 °C, 400 °C, 450 °C and 500 °C anneal respectively. Therefore, normality of the residuals assumption was considered to be valid at a significance level of α = 0.05 for rejecting the null hypothesis. The BF p-value was 0.58, therefore the assumption of variance homogeneity was considered to be valid at a significance level of α = 0.05. The Tukey pairwise comparison of the slope estimates had statistically significant differences between the 350 °C - 450 °C and the 350 °C - 500 °C

comparisons with p-values of 0.0285 and 0.005, respectively. Therefore, the anneal temperature has changed the slope of the linear regression after the 350 °C anneal and subsequently the sheet resistance of the p-GaN has changed. The current theory to explain this phenomenon is that the Mg has increased the doping of the p-GaN underneath the metal contact, leading to a reduction in the sheet resistance. This effect is not observed in the 3nm Mg sample, which could be explained by the theory that there was not enough Mg to contribute significantly to a reduction in the sheet resistance. Another consideration is the enthalpy of formation of any alloy between the Mg and Ni or Mg and Au that could be preferential to being substitiutionally included in the GaN lattice as a p-type dopant.The same Bonferroni procedure was used for making 6 comparisons of all the intercept estimates for the different anneal temperatures at an adjusted p-value = 0.00833. Testing the null hypothesis of H_0: β_1 - β_2 = 0, led to statistically significant differences between the intercept estimates between the 350 °C - 400 °C, 400 °C - 450 °C, 350 °- 450 °C and 350 °C - 500 °C treatments with p-values of 5.18×10^{-5}, 0.00458, 2.03×10^{-6} and 2.15×10^{-6}. Therefore, the anneal temperature had a statistically significant impact on the intercept estimates for the 350 °C, 400 °C and 450 °C treatments. A statistically significant difference in intercept estimates means that the contact resistance, R_C, and subsequently the transfer length, L_T, is different at these treatment levels. The theory of increased doping due to Mg inclusion underneath the ohmic contact is supported by the reduction in R_C and L_T. The 12nm Mg sample SW p-values were 0.46 and 0.27 for the 450 °C and 500 °C anneal respectively. Therefore, normality of the residuals assumption was considered to be valid at a significance level of α = 0.05 for rejecting the null hypothesis. The BF p-value was 0.79, therefore the assumption of variance homogeneity was considered to be valid at a significance level of α = 0.05. The p-value of the Tukey comparison between the two slope estimates had a p-value of 0.65. Therefore, the null hypothesis was accepted that the slope estimates are statistically identical for the two treatment. Testing the null hypothesis of H_0: β_1 - β_2 = 0, led to statistically insignificant differences between the intercept estimates between the two treatment levels with a p-value of 0.42. This observation suggests that there is a preferential thickness of Mg to include underneath the Ni/Au metals. Theories to explain this

phenomena are that the Mg becomes thick enough to set the barrier width at the interface and does not allow for Au diffusion to the p-GaN surface to occur. For the 20nm Mg sample, the SW p-values were 0.15, 0.28, 0.34 and 0.83 for the 350 °C, 400 °C, 450 °C and 500 °C anneal respectively. Therefore, normality of the residuals assumption was considered to be valid at a significance level of α = 0.05 for rejecting the null hypothesis. For the 20nm Mg sample, the BF p-value was 0.99, therefore the assumption of variance homogeneity was considered to be valid at a significance level of α = 0.05. The Tukey pairwise comparison of the slope estimates did not have any significant differences between treatment levels with the smallest p-value calculated at p = 0.95. The Bonferroni procedure for multiple comparisons between the intercept estimates did not have any statistically significant differences with the smallest p-value calculated at p = 0.64 between the 400 °C and 500 °C treatments. Again, this Mg thickness did not observe any significant difference in slope or intercept estimates which is the same conclusion reached for the 12nm Mg sample. These conclusions could be explained by the Mg layer being thick enough to limit the Au diffusion to the p-GaN surface. The microscope images shown in Figure 6.4 compare the color of different Mg thicknesses in the Ni/Au metal stack after a 500 °C anneal.

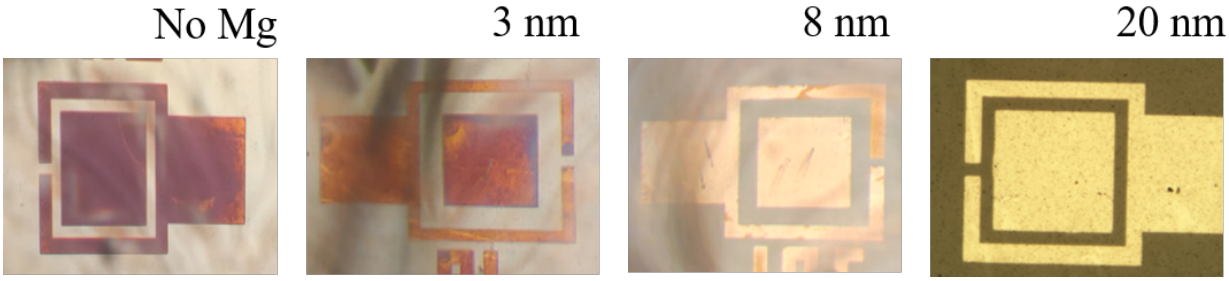

Figure 6.4: Microscope images after 500 °C anneal in Air for 5 minutes of the Ni/Au ohmic contacts to p-type GaN for different thickness of Mg included in the metal stack.

The change in color from the 0nm Mg sample from a golden/yellow color to purple after 500 °C anneal can be attributed to the Au diffusion to the p-GaN interface and the oxidation of the Ni to NiO. As the Mg thickness is increased, a difference in the color of the metal contacts is

observed after the anneal. For the 3nm sample, burnt orange/purple colors are observed which suggest that Au diffusion and Ni oxidation occurred. As the thickness is increased to 8nm, the contacts maintain the initial color but with areas of orange beginning to appear. This supports the theory that the Mg limits the Au diffusion to the interface and may react with the Ni to form Mg-Ni alloys that subsequently reduces the amount of Ni available for oxidation. Once the Mg thickness is increased above 8nm, there is no apparent change in color of the contacts after anneal. A summary of the specific contact resistivity values calculated for each Mg thickness and after each anneal is shown in Figure 6.8(a).

Secondary Ion Mass Spectroscopy (SIMS) was used to understand how the Mg and Ni are redistributed throught the metal contact and semiconductor after anneal at 500 °C. A Cs^+ ion beam at 14.5 keV, 5 nA and a $O_2{}^+$ beam at 4.5 keV, 50 nA was used to generate the following data. The contact pad size was 210 x 210 μm with the SIMS raster size of 80 x 80 μm inside the contact pad and a diaphragm used to capture an area of 50 x 50 μm to reduce detrimental cratering effects from the analysis technique. Analysis with a Caseium beam is shown, which is limited to observing MgO due to the electron affinity of Mg. Analysis with the oxygen beam enables tracking of elemental Mg. Due to limitations of the instrument, Au was not able to be monitored during the SIMS analysis. The results of the SIMS analysis for the baseline Ni/Au sample is shown in Figure 6.5. A strong oxygen signal is present at the top surface of the films due to the anneal being performed in an air ambient. The Ni signal is strong at the top surface of the film stack, which agrees with literature reports that Ni diffuses to the top surface to oxidize. The appearance of the substrate is monitored by tracking the GaN compound signal as shown in Figure 6.5. A relatively low concentration of Carbon is observed in the total film, suggesting proper vacuum deposition conditions for the evaporated Ni. However, a Carbon peak at the interface of the GaN and Ni is present which is expected due to the substrate being exposed to ambient before deposition of the Nickel film. The $O_2{}^+$ beam shows a background signal of Mg in the GaN films, were the Nitrogen signal is used to determine when the substrate is reached. Nickel has diffused to the top surface and is diffused throughout the film stack.

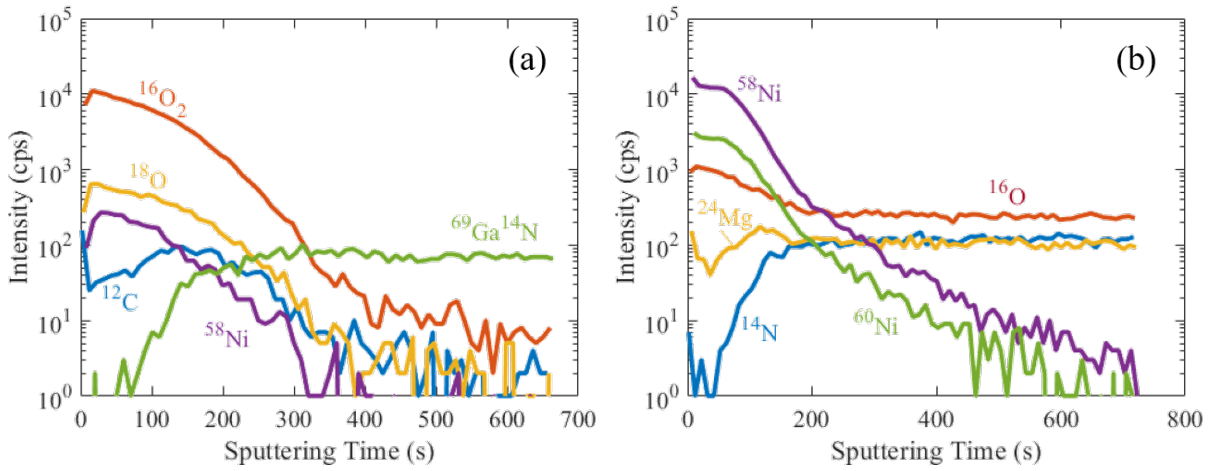

Figure 6.5: SIMS plot using a (a) Cs^+ and (b) O_2^+ ion beam for the baseline sample with 25 nm Ni and 25 nm Au after 500 °C anneal.

The SIMS profile for the 8 nm Mg sample after 500 °C anneal is shown in Figure 6.6. Similar to the baseline Ni/Au sample a strong peak of oxygen is observed throughout the film stack, suggesting that the metals have oxidized due to the anneal in air ambient. Interestingly, a strong MgO signal is present throughout the film stack which suggests that like the Ni, the Mg is diffusing towards the top surface to oxidize. The Ni signal shows that it too has diffused to the surface to oxidize as was the case with the baseline Ni/Au sample. Again, the Carbon signal intensity is low throughout the film structure but a peak is observed at the top surface and at the interface with the GaN. As a vacuum break was required between the Mg/Ni deposition and the Au sputter this is acceptable for a peak of Carbon near the top surface. As with the baseline Ni/Au sample, a Carbon peak is observed at the interface of the GaN which is attributed to the substrate being exposed to ambient before Mg/Ni deposition. An isotope of Mg is tracked to verify the presence of MgO and aid in the differentiation between MgO and C_2O. The present SIMS profiles suggest that Mg and Ni have both diffused to the surface to oxidize.The O_2^+ beam data shows two peaks of Mg, one at the top surface of the film and another at the interface of the p-GaN. This verifies that the Mg has diffused to the top surface to oxidize and also stays at the semiconductor interface where it can contribute to doping.

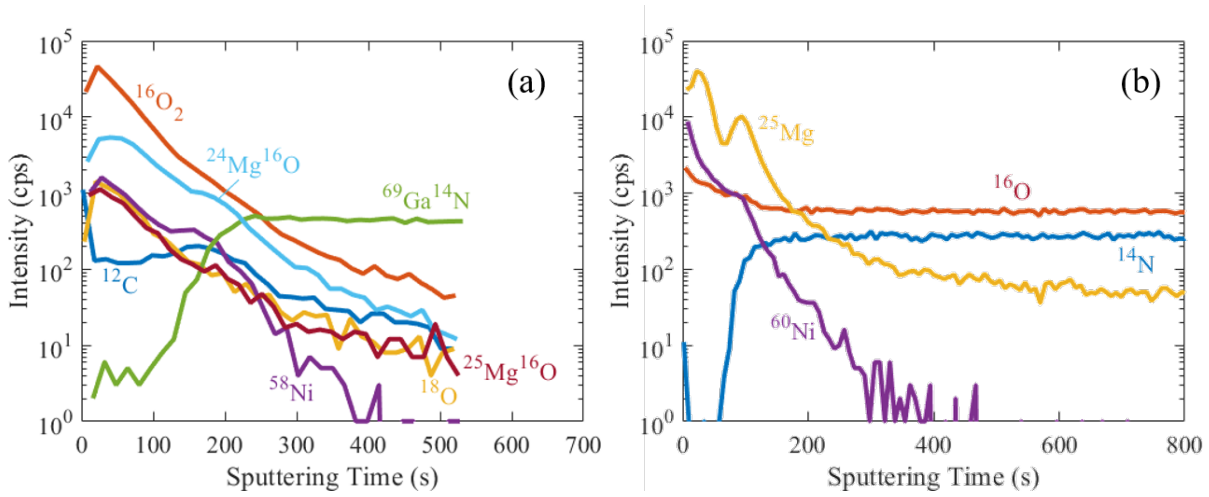

Figure 6.6: SIMS plot using a (a) Cs^+ and (b) $O_2{}^+$ ion beam for the 8 nm Mg sample with 25 nm Ni and 25 nm Au after 500 °C anneal.

The SIMS profile for the 20 nm Mg sample after 500 °C anneal is shown in Figure 6.7. Similar to the previous two SIMS profiles, a strong concentration of oxygen is present throughout the film stack due to anneal in ambient. However, a strong peak of MgO and Ni is observed near the top surface of the metal stack. Specifically the strong peak of Ni at the top surface of the metal stack suggests that the Mg is restricting the Ni from oxidation.

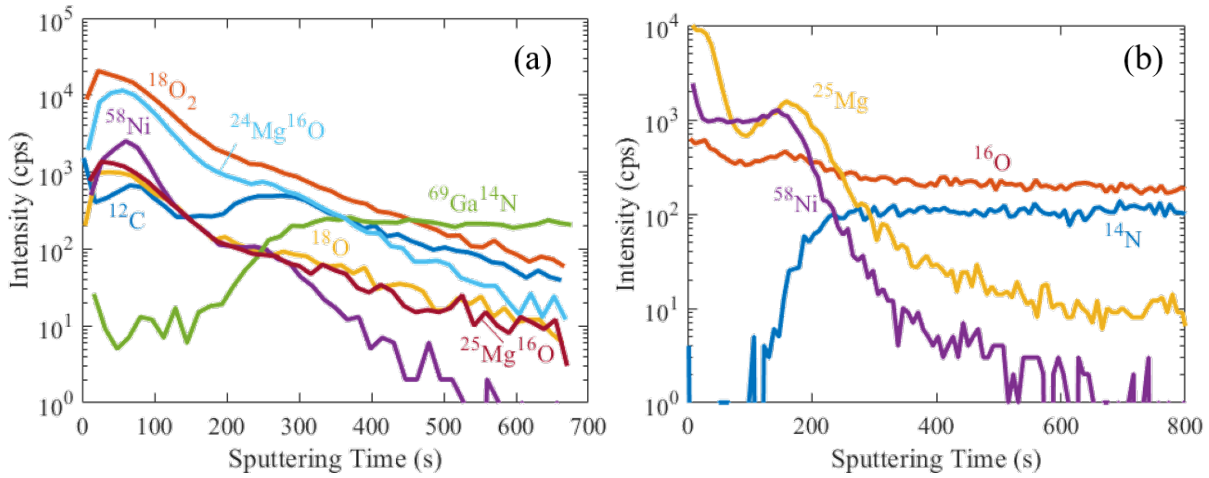

Figure 6.7: SIMS plot using a (a) Cs^+ and (b) $O_2{}^+$ ion beam for the 20 nm Mg sample with 25 nm Ni and 25 nm Au after 500 °C anneal.

This hypothesis is supported by the O_2^+ beam data that shows a uniform thickness of Ni still present in the metal stack. Whereas the other two samples showed a diffused Ni profile. A larger peak of Mg is present at the semiconductor surface compared to the 8 nm sample. This extra Mg could control the effective work function present at the metal-semiconductor junction, leading to a reduction in specific contact resistivity. Literature reports suggest that the oxidation of Ni is critical to forming a low resistance ohmic contact to p-GaN. This observation supports the hypothesis that too much Mg included in the metal stack leads to a reduction in specific contact resistivity. Furthermore, this suggest that there is an optimal amount of Mg to include the metal stack, where too little leads to a negligible difference in contact resistivity but too much inhibits the oxidation of the Ni films.

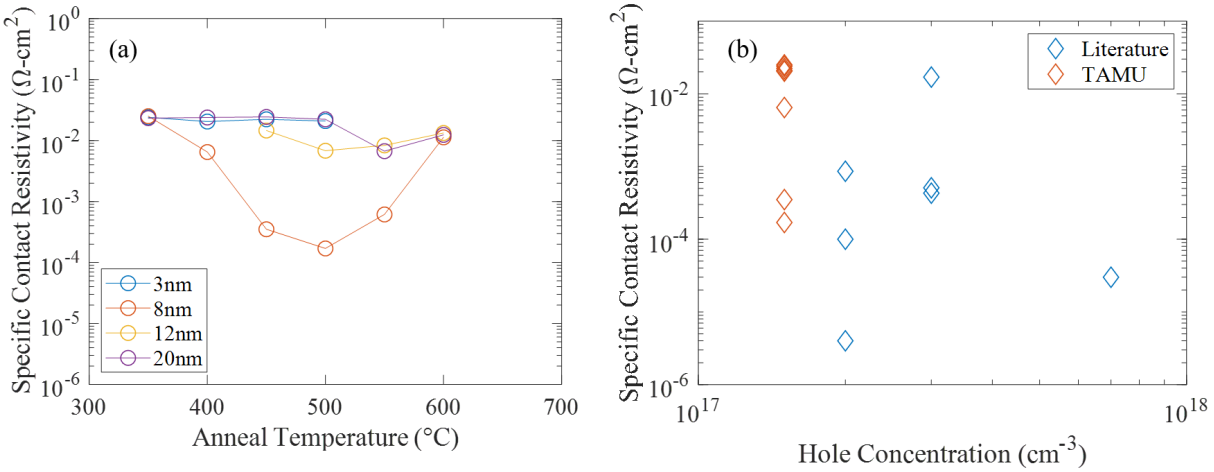

Figure 6.8: (a) Summary of the Mg/Ni/Au study plotting the specific contact resistivity versus anneal temperature. (b) A comparison of the work completed herein to literature.

The 3nm, 20nm and 12nm Mg samples did not show a statistically significant change in ρ_C with different anneal temperatures. However, the 8 nm sample did show significant changes in ρ_C with increasing anneal temperature. The results of this study are compared to literature reports as shown in Figure 6.8(b). The comparison of the results presented herein are not the best reported to date. It is possible that if the doping density of the starting material was higher or all three metals

could be deposited in-situ that these results could improve. Future experiments could include in-situ deposition of all the metals, using different thicknesses of the Ni/Au stack to study their impact on the metal stack.

7. CONCLUSION & OUTLOOK

A parametric study of design criteria and processing conditions for GaN SJs has been presented. Interestingly, the GaN SJ is more robust to charge imbalance between SJ columns when compared to Silicon SJs. Specifically, doping the n-GaN column higher than the p-GaN column(s) can improve V_{BR}. Furthermore, diffusion of dopants, such as Magnesium and Silicon, do not affect V_{BR} and R_{ON} significantly. This study suggests that the critical design parameters are the total charge per SJ column and the specific contact resistivity of the metal-semiconductor junctions. With conservative contact resistivities to the N+ and P+ regions of the SJ, a FOM comparable to commercial GaN devices is obtainable. Wurtzite GaN was successfully grown on an ALD Al_2O_3 buffer layer on Silicon (111) and (100) substrates. The crystal quality of the two GaN films followed a similar trend with thickness of the ALD Al_2O_3 layer. While the crystal quality between the two films was signficantly different, diodes fabricated from the two films were not drastically different. The sheet resistance of the GaN-on-Silicon (100) substrates was approximately 6x lower than the GaN-on-Silicon (111) films, but interfacial impurities limited the current observed in the GaN-on-Silicon (100) schottky diodes. These results suggest that high quality GaN-on-Silicon (100) could be manufactured with an improved film quality. A GaN-on-Sapphire process was developed and met the XRD FWHM goals as shown in Table 7.1.

Metric	Goal	GaN SJ
Window Aspect Ratio	> 1	1.2
GaN XRD FWHM (002)	< 500 arcseconds	309 arcseconds
n-GaN R_C	$< 10^{-5}\ \Omega - cm^2$	$2.1\text{x}10^{-6}\ \Omega - cm^2$
p-GaN R_C	$< 10^{-4}\ \Omega - cm^2$	$1.7\text{x}10^{-4}\ \Omega - cm^2$
Diode R_{ON}	$< 5\text{x}10^{-3}\ \Omega - cm^2$	N/A
Diode V_{BR}	> 200 V	N/A

Table 7.1: Goals and results for the research presented herein.

An ART process was developed using EBL and RIE to allow for 100 nm wide windows to be etched in a Si_3N_4 masked used for SAE of GaN. The aspect ratio of the windows was 1.2, which allows trapping of defects before extending beyond the window. These results were confirmed with TEM. Ohmic contacts to n-GaN and p-GaN were developed with specific contact resistivities listed in Table 7.1. A Mg inter-layer was added between the p-GaN surface and Ni/Au metal stack typically used for making low resistance contacts to p-GaN. The inclusion of Mg improved the contact resistivity by > 100x, but was only observed for 8 nm of Mg. Thinner and thicker Mg layers appeared to have no affect on the specific contact resistivity.

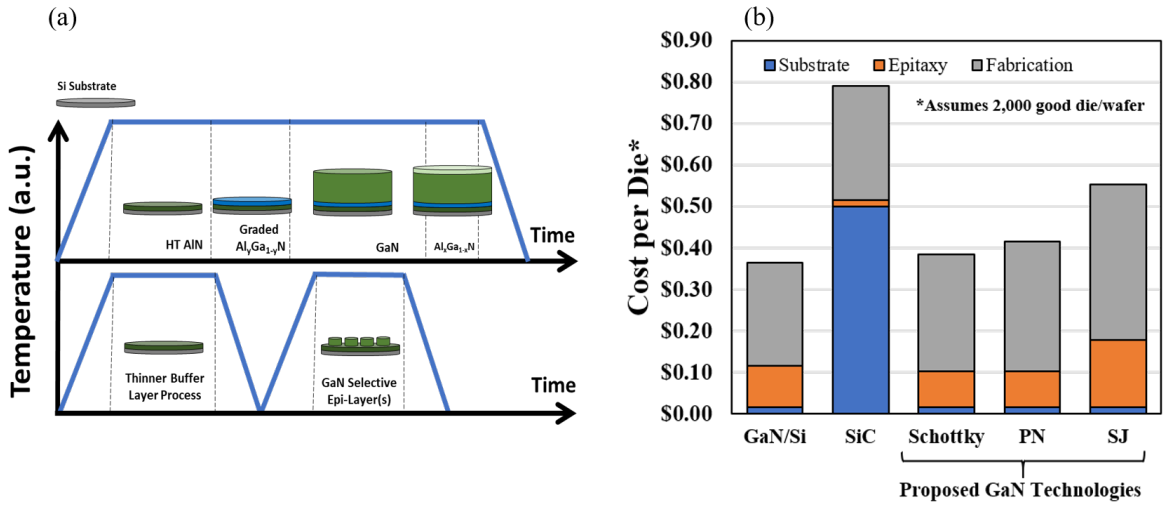

Figure 7.1: (a) MOCVD growth time for the Schottky proposed GaN technology (b) cost analysis for 150mm wide-band gap technologies and the proposed GaN technologies

The proposed manufacturing process requires many re-growths and can be costly if no modifications to a standard GaN process flow are implemented. Therefore, it is proposed in Figure 7.1(a) that a thinner buffer layer process could be employed to allow for larger wafer diameters and to help reduce the additional MOCVD growth time required to realize a GaN SJ. The higher growth rate of the SAE process will allow for shorter deposition times for the three re-growths necessary to manufacture the proposed GaN SJ. Ramp times will contribute to a significant amount of ad-

ditional time and should be considered accordingly. A cost analysis is shown in Figure 7.1(b) for three possible technologies that are based on the processes developed herein. The Schottky process enables the greatest cost savings relative to the SiC technology, while still being cost competitive with current GaN/Si technology. However, as the fabrication process becomes more complex, it is clear that the proposed technology is more expensive than current GaN/Si. Therefore, devices fabricated that utilize SAE and/or ART will need to provide significant performance improvements to account for the increased manufacturing costs.

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APPENDIX A

SUPERJUNCTION SIMULATION COMMAND FILE

```
********** FILE **********
File {
*input files
Grid= "GaNSJ1200V_msh.tdr"
Parameter= "models_GaN.par"
*output files
Plot= "GaNSJ_des.tdr"
Current= "GaNSJ_des.plt"
Output= "GaNSJ_des.log"
}
********** ELECTRODE **********
Electrode {
{ Name="anode" Voltage= 0}
{ Name="cathode" Voltage= 0}
********** PHYSICS **********
Physics {
Hydrodynamic(eTemperature)
Mobility(
DopingDependence
eHighfieldsaturation(GradQuasiFermi) )
EffectiveIntrinsicDensity (Nobandgapnarrowing)
Piezoelectric_Polarization (strain)
Piezoelectric_Polarization (stress)
```

Recombination(

SRH

Avalanche(ElectricField)

)

Fermi

RecGenHeat

Aniso(Poisson) }

Physics (Material="GaN")

Plot { Potential Electricfield/Vector PE_Polarization/vector PE_Charge eDensity hDensity eCurrent/Vector hCurrent/Vector TotalCurrent/Vector SRH Auger Avalanche eMobility hMobility eQuasiFermi hQuasiFermi eGradQuasiFermi hGradQuasiFermi eEparallel hEparallel eMobility hMobility eVelocity hVelocity DonorConcentration Acceptorconcentration Doping SpaceCharge ConductionBand ValenceBand BandGap Affinity xMoleFraction eTemperature hTemperature eTrappedCharge hTrappedCharge eIonIntegral hIonIntegral MeanIonIntegral eAlphaAvalanche hAlphaAvalanche *for breakdown

}

Math Extrapolate Iterations= 40 Digits = 6 ErrRef(electron) = 1E5 ErrRef(hole) = 1E5 RHSmin= 1e-10 RHSmax= 1e30 CDensityMin= 1e-20 DirectCurrentComputation RelTermMinDensity= 1e5 eMobilityAveraging= ElementEdge ComputeIonizationIntegrals BreakAtIonIntegral(3 1.)

Solve

Coupled (Iterations= 100000 LinesearchDamping= 0.001) Poisson Coupled (Iterations= 100) Poisson Electron Hole

********** I-V SWEEP **********

solve initial conditions Poisson Coupled Poisson Electron Coupled Poisson Electron Hole Save (FilePrefix="vi0")

minimum anode voltage Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.5 Goal Name="anode" Voltage=0) Coupled Poisson Electron Hole Save(FilePrefix="diode_iv")

Load(FilePrefix="diode_iv") NewCurrentPrefix="diode_iv_" reverse bias Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.05 Goal Name="anode" Voltage=5) Coupled Poisson Electron Hole

NewCurrentPrefix="diff1200Vdiode100_" Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.1 Goal Name="cathode" Voltage=100) Coupled Poisson Electron Hole

NewCurrentPrefix="diff1200Vdiode200_" Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.5 Goal Name="cathode" Voltage=300) Coupled Poisson Electron Hole

NewCurrentPrefix="diff1200Vdiode500_" Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.1 Goal Name="cathode" Voltage=500) Coupled Poisson Electron Hole

NewCurrentPrefix="diff1200Vdiode1000_" Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.1 Goal Name="cathode" Voltage=1000) Coupled Poisson Electron Hole

NewCurrentPrefix="diff1200Vdiode1300_" Quasistationary (InitialStep= 1e-3 Minstep= 1e-7 MaxStep= 0.1 Goal Name="cathode" Voltage=1300) Coupled Poisson Electron Hole

APPENDIX B

SUPERJUNCTION MANUFACTURING PROCESSES

Text for the Appendix follows.

B.1 Process Number 2

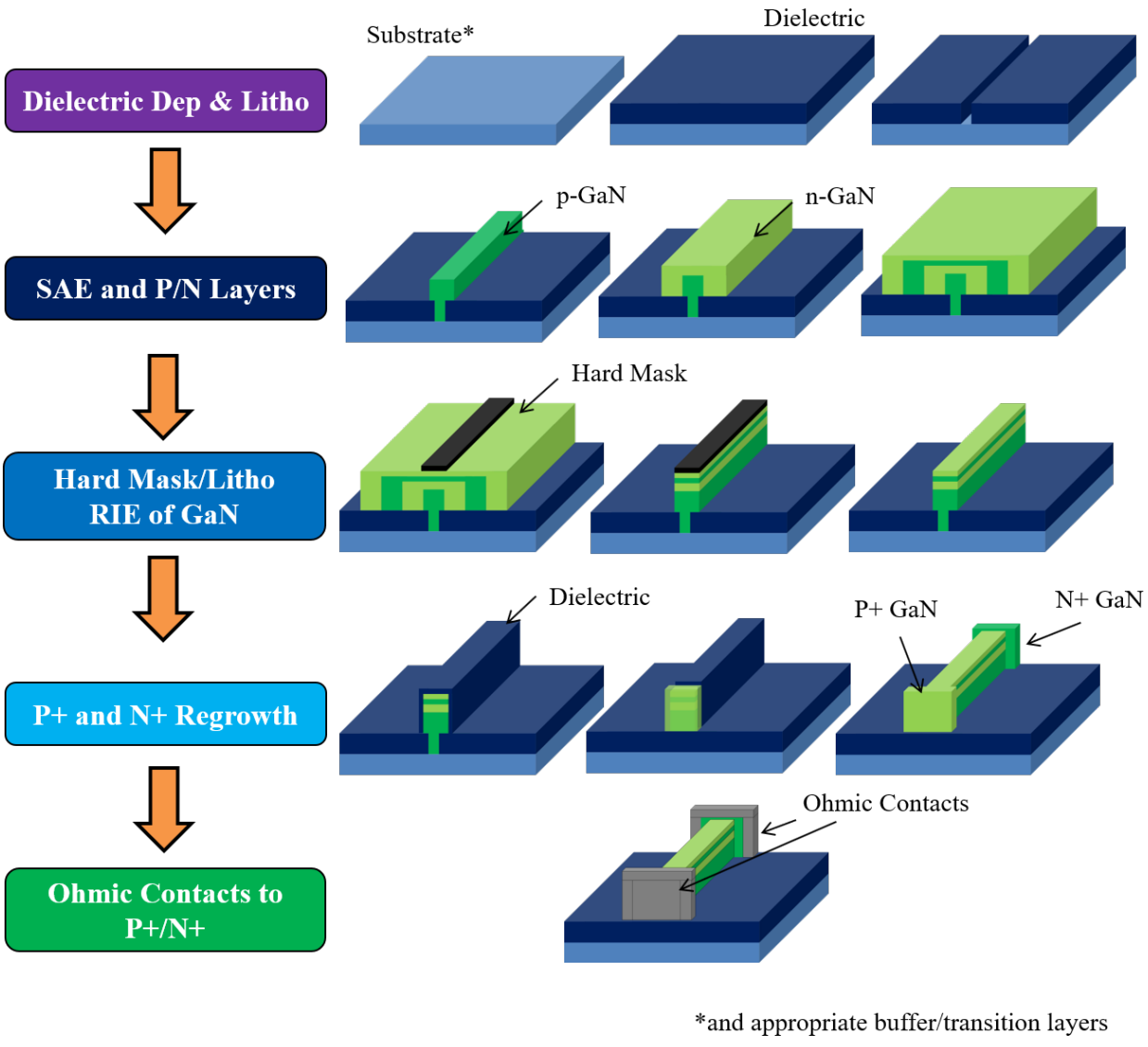

Figure B.1: Process 2 for fabricating Lateral Superjunctions.

B.2 Process Number 3

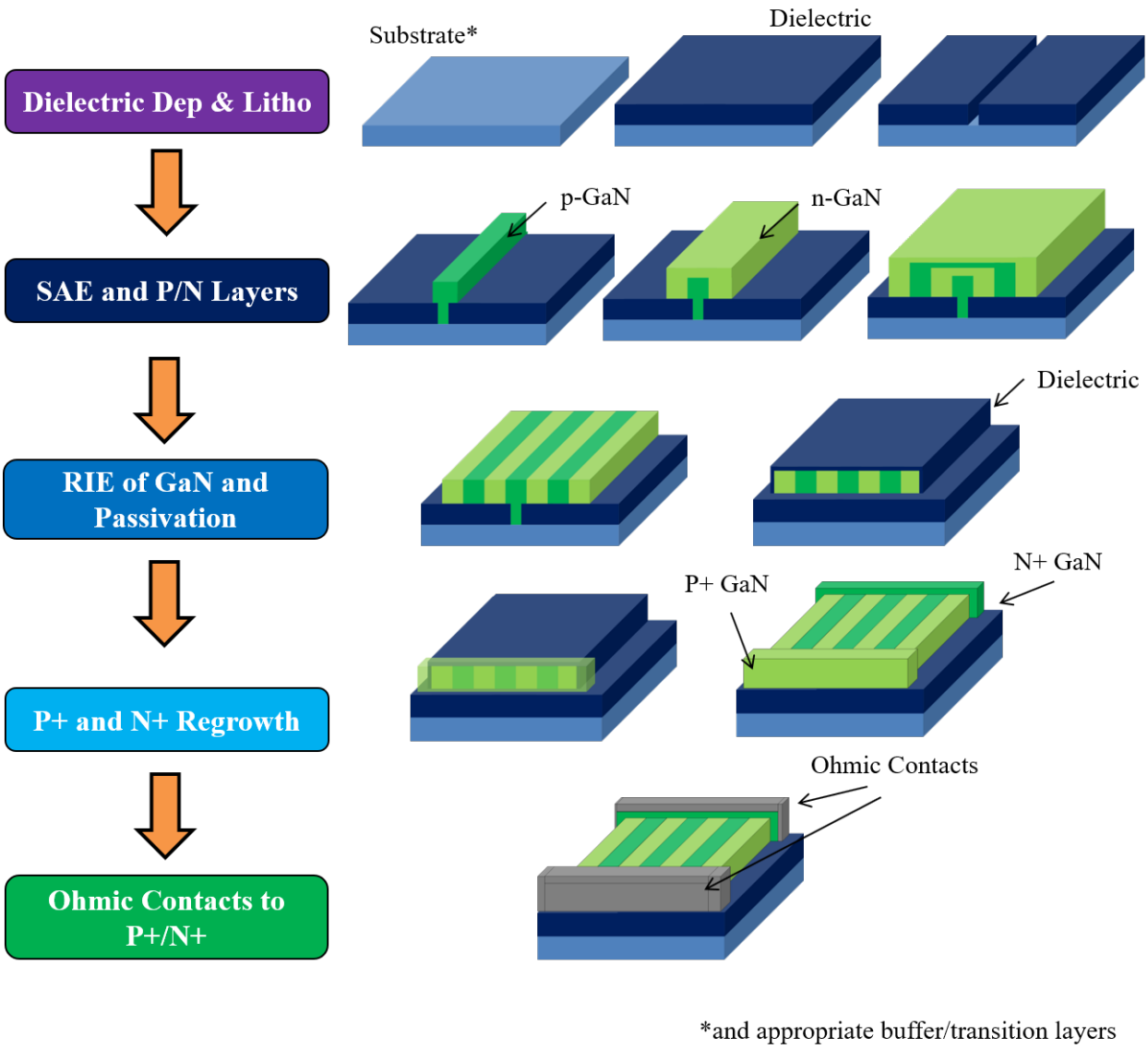

Figure B.2: Process 3 for fabricating Lateral Superjunctions.